

**DEVELOPMENT OF A  
CALL ALERT SYSTEM  
FOR PAGING MINE PERSONNEL**

John Trombly, Program Director  
Stuart Lipoff, Paul O'Brien

*prepared for*

**UNITED STATES  
DEPARTMENT OF THE INTERIOR  
BUREAU OF MINES**

*by*

**ARTHUR D. LITTLE, INC.  
CAMBRIDGE, MASSACHUSETTS**

**FINAL REPORT**

**On Contract No. HO 262026**

Arthur D. Little, Inc.

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FOR PAGING MINE PERSONNEL

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<p>16. Abstract</p> <p>System objectives and design criteria for an in-mine ULF radio paging system are discussed. Coding formats, frequency and bandwidth selection criteria leading to the system design are discussed. The prototype call alert transmitter and pocket page receiver is functionally described. The report includes circuit descriptions, schematics, parts lists, printed circuit fabrication and assembly drawings. The report concludes with an estimate of the manufacturing cost for each assembly.</p>			
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## FOREWORD

This report was prepared by Arthur D. Little, Inc., Cambridge, Massachusetts under USBM Contract No. H0262026. The contract was initiated under the Coal Mine Health and Safety Program. It was administered under the technical direction of the Pittsburgh Mining and Safety Research Center with Mr. Harry Dobroski acting as the technical project officer. Mr. George Honold was the contract administrator for the Bureau of Mines.

This report is a summary of the work recently completed as part of this contract during the period June 1976 to June 1977.

No inventions or patents were developed and no applications for inventions or patents are pending.

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## I. INTRODUCTION AND SUMMARY

### A. OBJECTIVE

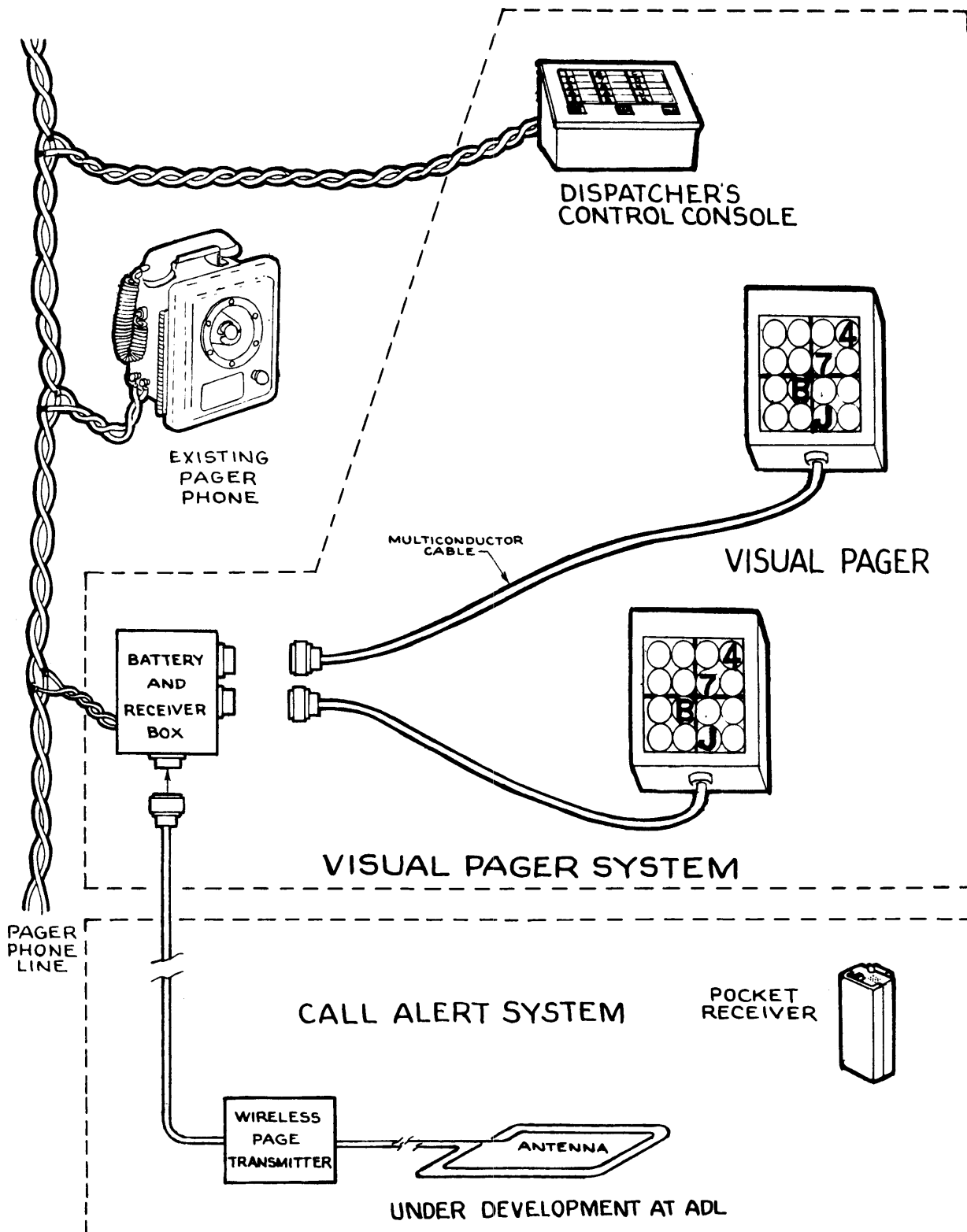
For a number of years, coal mines small and large have made extensive use of party line pager telephones to communicate into and between working areas as well as to supervisory sites above and below ground. These phones page the callee by means of a self-contained loudspeaker; normal communications are then carried on by a conventional telephone hand set. The acquisition range depends on how audible the speaker is, as well as on the number of phones in a given area, and the chances of a callee being in their vicinity.

Clearly, there are operational drawbacks to the system. To remedy these, the use of visual pager units has been proposed, and engineering models of such units are currently under development. These, in their simplest form, are display panels which, when selectively activated, show symbols to designate paged individuals who have not been reached via the voice paging system.

These display panels enlarge the paging area and can be installed where phones are not needed. Unless these display panels are read by all concerned, they too, like the pager phone will sometimes fail to notify an individual that he is being paged.

The ultimate system is a wireless scheme which can selectively page any one of a number of miniature pocket receivers carried by key mine personnel; thereby providing each of these individuals with a personal alerting signal that he should call in. Such wireless schemes can cover a large working area, and are almost impossible to ignore.

From a system engineering point of view, all three paging techniques: phone, visual, and wireless perform basically the same function; and they benefit greatly by being made modules of a complete paging system which uses any or all three modes of communication. Figure 1 illustrates the system concept. This shows the existing pager phone hardware, the visual pager hardware developed by ADL for the Bureau, and the additional equipment necessary to add the wireless page capability.



**BLOCK DIAGRAM  
CALL ALERT SYSTEM  
WITH PROTOTYPE VISUAL PAGER**

Figure 1

The objective as outlined in this figure is to provide an add-on wireless pager system that is fully compatible with the existing voice pager phone equipment and with the visual paging system previously developed.

#### B. SYSTEM DESCRIPTION

The call alert system, as delivered to the Bureau of Mines, is comprised of three prototype pocket page receivers, a compact page transmitter and an interconnecting cable to interconnect a visual display with the transmitter. The system can be expanded, without modification, to page a total of 15 receivers and then the capacity of the system is only limited by the visual pager's dispatcher's console. The pocket receivers, shown in Figure 2, are designed to accommodate 32 distinct codes without modification. If the design capacity is perceived to be a limiting factor, the receivers can be expanded to a field of 128 codes with only a very minor modification.

The receiver, as depicted in Figure 2, is completely self-contained. The enclosure houses a ferrite loop antenna, aural and visual alarms, two printed circuit cards and a rechargeable nickel cadmium battery designed to provide approximately 40 hours of continuous service between charges. Two contacts are provided at the bottom of the receiver for charging from a 12-volt source.

When the receiver is switched on, the aural alarm sounds to indicate to the wearer that the batteries are charged and the receiver is operational. If a page is received corresponding to the code stored in the receiver, the aural alarm sounds for about 2 seconds and the light emitting diode illuminates steadily. The LED can be reset by depressing the slide switch.

The receiver's address code is programmed by inserting wire bridges in a header located on the upper printed circuit card. This dip header is visible in the upper left-hand portion of the disassembled receiver in Figure 2.

The call alert transmitter is shown in Figure 3. The enclosure houses a wire wrapped card assembly, rechargeable battery and a switch panel

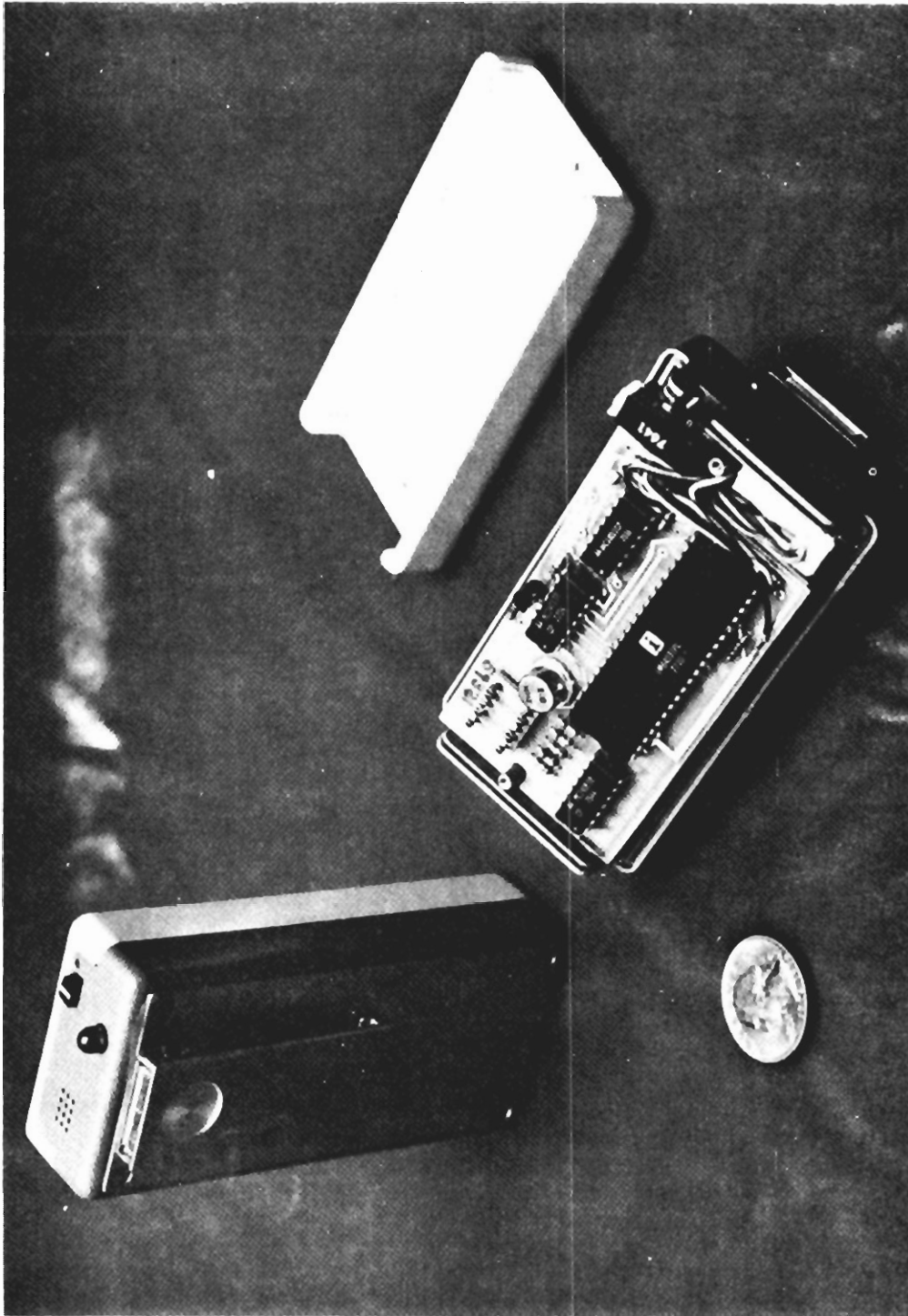


Figure 2

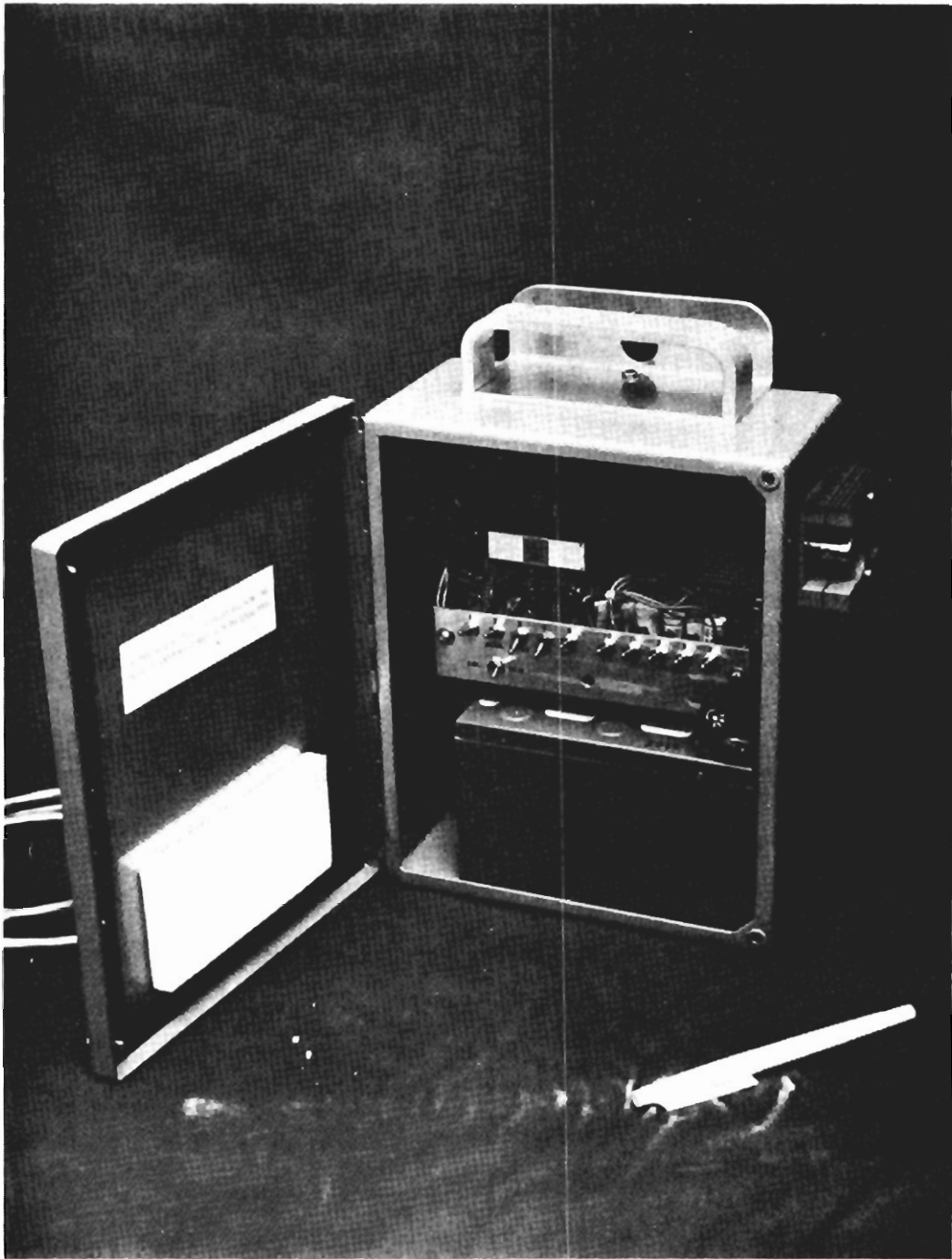


Figure 3

for installation and system test. The transmitter can be operated on a stand-alone basis, completely independent of the visual pager system for test purposes. In normal operation, however, the transmitter is controlled by a dispatcher's console, using an existing pager phone line as a communications link. The transmitter derives decoded signals by plugging into a standard visual display or a battery/receiver box such as shown in Figure 1.

The transmitter's battery is designed to accommodate up to 7,000 pages between charge cycles. As the battery is depleted, the transmitter loses power without disabling the visual display that the transmitter may be interfaced with.

The transmitter may be controlled manually from a switch panel, pictured in Figure 4, located just inside the hinged front cover. The switch panel permits code selection, antenna tuning and remote/local control.

#### C. FINDINGS AND CONCLUSIONS

The call alert system has been successfully demonstrated at the ADL building complex and grounds as well as at the Bureau of Mines test mine in Bruceton. The primary performance criteria for a paging system are, of course, paging range and falsing rate, particularly when the receiver is operating in an area of intense electromagnetic interference. The paging range meets with our original system goals of 500 to 1000 feet as a function of surrounding strata and electromagnetic noise. Typical paging range at the Bruceton mine was estimated to be 700 feet, according to the Technical Project Monitor.

One false page was detected during controlled tests at Bruceton, but only while the transmitter endlessly repeated a specific code. Since the test was conducted during a 20 minute period, during which 2,200 pages were transmitted; one false page is equivalent to a falsing rate of one every 73 days if 30 pages per day is assumed to be a typical radio paging rate.

The call alert receiver is most susceptible to falsing at the fringe of a signalling area and only if the receiver passes through a field below the receiver's capture range during the course of the page. Both

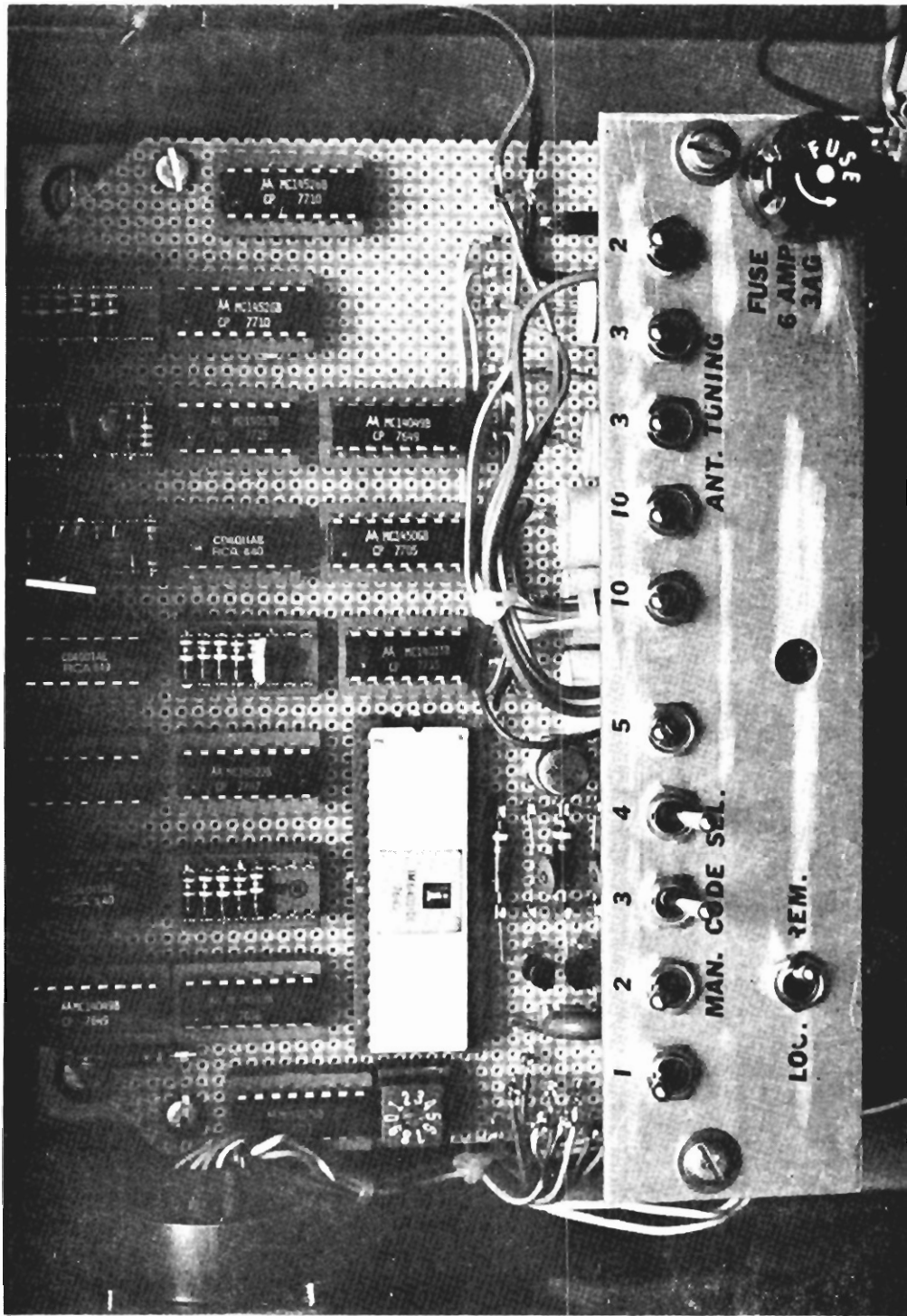


Figure 4



conditions must occur since not only must the receiver synchronize with the incoming data stream, but the code must match the five bit code stored by the receiver. In addition, parity and framing conditions must be met.

In addition to paging performance, system goals emphasized design of a compact lightweight and rugged paging receiver. Figure 2 clearly indicates the small size of the receiver, made possible by extensive use of LSI technology, without resorting to hybrid circuits or other manufacturing techniques not commonly employed by the mining communications industry.

## II. THE CALL ALERT SYSTEM

### A. BACKGROUND

Since the choice of an operating frequency based upon field tests was beyond the scope of this project, the 3 kHz band currently in use by Collins Radio was selected to minimize contingencies. It is believed that this band offers the advantage of optimum range traded against the disadvantages of high ambient noise and large physical antenna size. It is further hypothesized that the use of this low frequency will permit a simple, low power and low cost receiver design.

Conventional radio paging receiver modulation schemes have employed baseband modulation of audio tones onto the carrier frequency. Size and cost economies in these state-of-the-art pagers have employed mechanical tuning fork filters in the audio frequency range of 300 Hz - 3 kHz. These conventional baseband audio tone techniques were judged to be unsuitable for our Call Alert System. At a carrier frequency of 3 kHz, baseband tone modulation of even 300 Hz would require such a large relative occupied bandwidth about the 3 kHz carrier, that the system range would be expected to suffer. Furthermore, the use of mechanical filters which are sensitive to shock is not compatible with the mine environment. The use of audio tone frequencies below 300 Hz with active filter techniques is possible, but the large physical size and high cost requirements of the required capacitors make this approach unattractive. Furthermore, the signalling time per page for these low frequency tones may be expected to be substantial.

Digital coding schemes on the other hand offer flexibility in system performance; permitting sensitivity, code set size, signalling time, and falsing performance to be easily traded off against one another. In addition, digital decoders permit straightforward homogeneous integrated circuit custom designs which in turn enhance size and current drain performance.

Phase Shift Keying (PSK) is a special case of FSK that is ideally suited for this application. By choosing the differential scheme shown in

Figure 5, the modulator is easily implemented and the demodulation process is straightforward, provided phased-lock loop techniques are employed to recover the data. The coherent demodulation provided by the phase-locked loop insures maximum system range as predicted by signal detection theory. Furthermore, PSK provides an approximate 6 dB reduction in required received power for the same CW system performance.\*

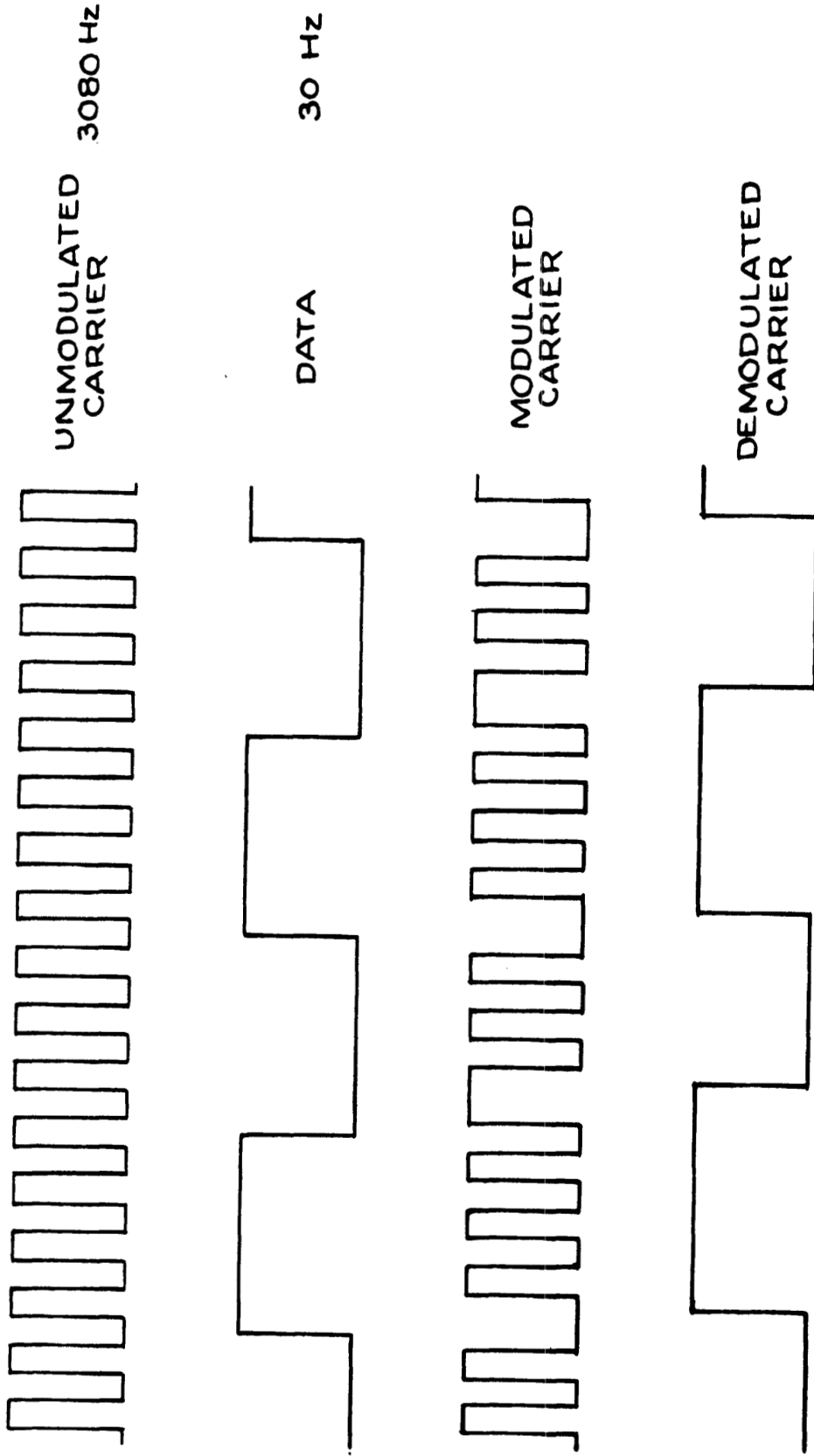
The occupied bandwidth required by the signal of Figure 5 was measured using a synchronous modulator connected to an HP3580A spectrum analyzer. The modulator input signal consisted of a 50% duty cycle square wave of modulation frequency 3, 30, and 300 Hz. The spectrum analyzer photographs are attached as Figures 6, 7, and 8. Figure 9 is a photograph of an unmodulated carrier for reference. Note the following features of the spectrum: The carrier frequency is nulled out, the first set of sidebands is +/- the modulation rate and 4 dB down from the carrier, the other sidebands are spaced multiples of the modulation rate and fall off rapidly with increasing spacing from the carrier. To a good approximation, the occupied bandwidth is equal to four times the modulation rate. In general, the carrier will not disappear for a modulation bit stream with a duty cycle different from 50%; but in this case, the occupied bandwidth will also be less so the above approximation is a good upper bound.

The 30 Hz modulation rate has an occupied bandwidth of 120 Hz and thus would permit the carrier and its modulation products to be placed between the 180 Hz 3-phase power line harmonic noise prevalent in the mines. The 30 Hz data rate permits an eight bit serial word to be transmitted in about 260 ms, not an unreasonable delay in comparison to a dispatcher's keying interval when operating the console.

The system protection against false alarms will, to a large extent, determine the acceptance of the system by the users. Commonly used rates for com-

---

\*Bennett and Davey, Data Transmission, McGraw-Hill, New York City, 1965.



DIFFERENTIAL PHASE SHIFT KEYING

FIGURE 5

Occupied Bandwidth of Differential PSK Modulation  
Vertical Amplitude Scale is 1 dB/Div

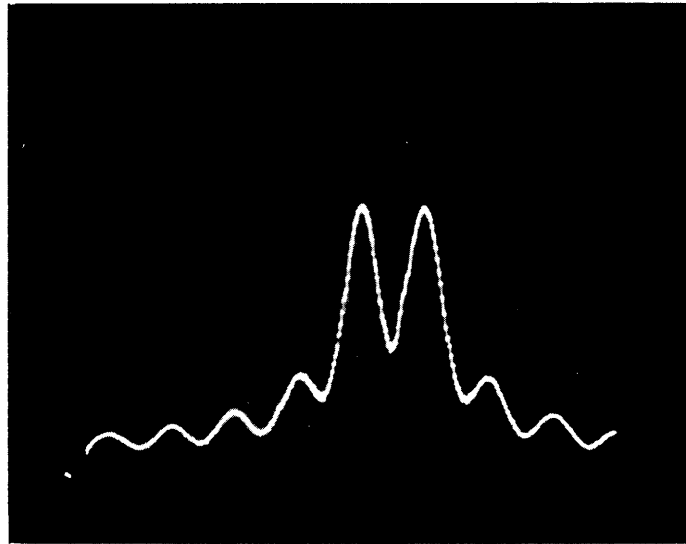


Figure 6  
Modulation Rate 3 Hz, Horizontal Scale 5 Hz/Div

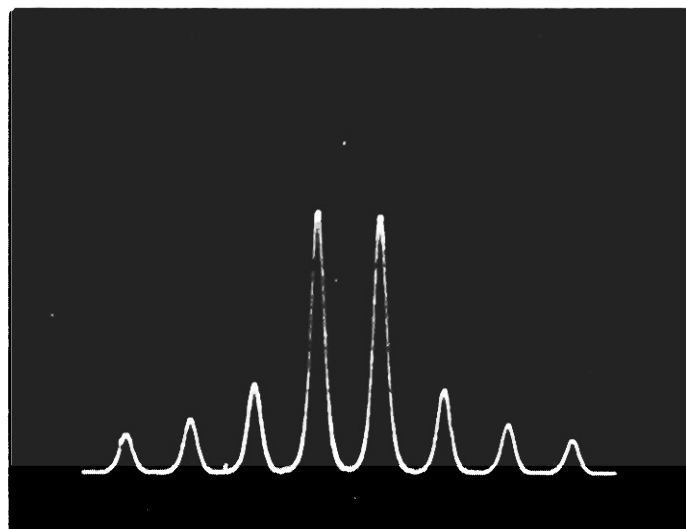


Figure 7  
Modulation Rate 30 Hz, Horizontal Scale 50 Hz/Div

Vertical Amplitude Scale is 1 dB/Div

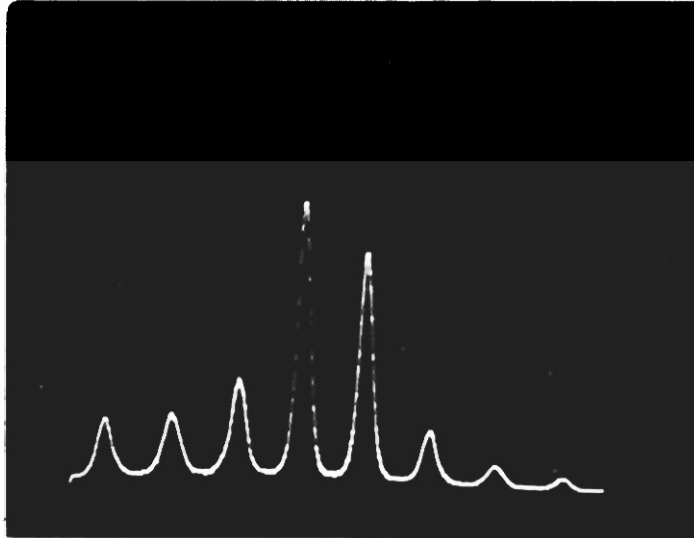


Figure 8  
Modulation Rate 300 Hz, Horizontal Scale 500 Hz/Div

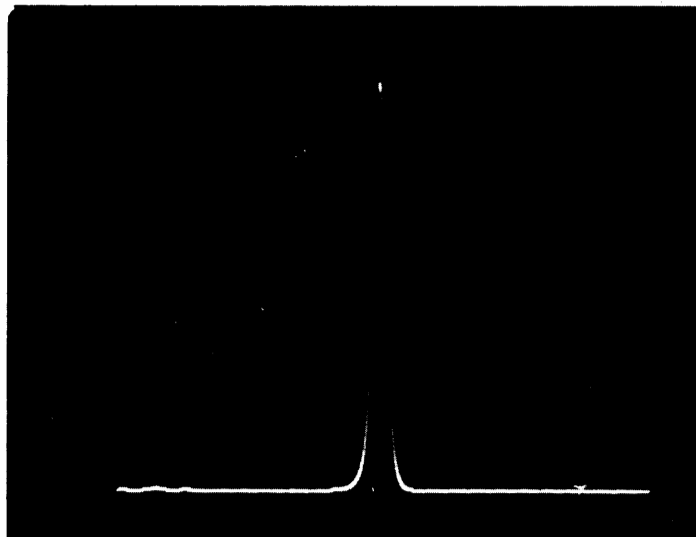


Figure 9  
Unmodulated Reference

mercial radio common carrier paging should also apply to the mining application. Industry standard limits are 0.1% falses per total pages transmitted. The system design should insure that falsing rates for random noise falsing are not significant compared to single bit falsing on a valid page intended for another pager.

#### 1. Page Queuing

While posting a sequence of pages in the Visual Pager system, a fleet-fingered dispatcher could post pages at the maximum system rate of 200 ms per page. Consequently, a queuing delay occurs while the transmitter serially outputs a page. A visual pager processes the data in real time and therefore has no need to store the pages. The burden for storing pages as they are generated by the dispatcher is placed on the Call Alert transmitter.

When viewed from a systems perspective, four solutions to page queuing appear feasible. In the first approach the length of the pager code could be shortened to a total of six bits to dispose of the delay. The field of addresses would be reduced to about four unique codes. Although as few as four addresses may be sufficient to evaluate the Call Alert System, no flexibility is provided for future expansion.

The second approach considered would retain the aforementioned data rate but would only store the current page for transmission. The transmitter's input port would go into a busy mode while a page is transmitted and additional pages posted by a dispatcher would be ignored, until the current transmission is completed. Since considerable time could expire between pages, this approach offers a reasonable tradeoff.

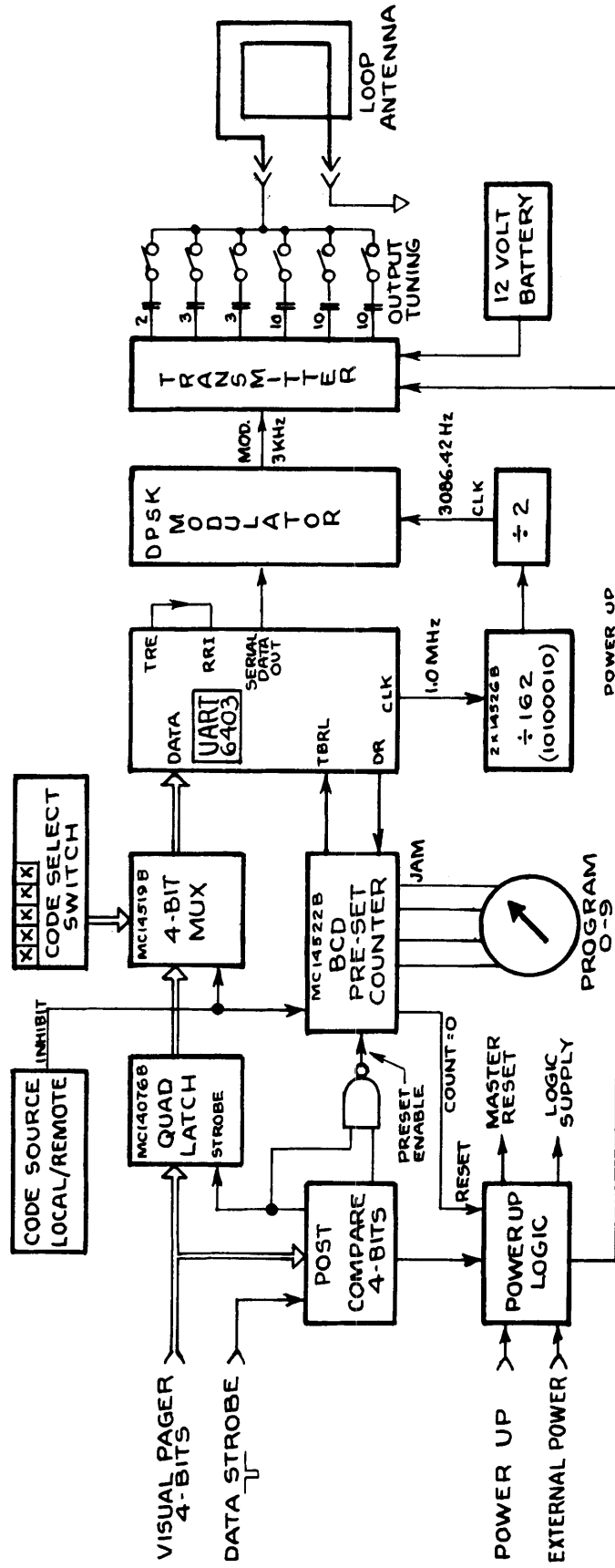
The third approach considered would store all of the pages as they were posted by the dispatcher. The capacity of the memory would permit the entire roster of 15 possible pages to be stored in the sequence of their posting. The transmitter would serially step through the memory stack until it arrived at a page for transmission. The page would be transmitted and a portion of the memory reserved to count the number of times that page was outpulsed would be incremented. If the page

was incremented  $n$  times, where  $n$  in this case is equal to perhaps 5, it would be erased from the memory stack. Following a page cycle, the transmitter would step to the next page in sequence in the stack. If the dispatcher repeated the posting of a page still current in the stack, the counter would be reset to  $n = 0$ , rather than re-entering the page. The contents of the memory would not overflow with the repeated entry of the same page. When the transmitter completes outpulsing of all pages currently in the stack, power would be switched off until a new post command is received from the dispatcher.

The last approach considered is a truncated form of the processing scheme described above. Rather than storing the entire field of 15 possible pages, only two pages are stored. One is currently being transmitted while the second page, if it is posted, is stored. Each page is repeatedly transmitted, as described earlier. If a third page is posted sequentially, then the first page received by the Call Alert transmitter is bumped. It should be noted here that this arrangement permits a reasonable probability of transmitting at least three sequential pages, even at the hands of a fleet-fingered dispatcher. As the dispatcher keys the third page, 600 ms have elapsed, so the first page has already been transmitted. The disadvantage, of course, is clear. The first page is bumped and therefore is only transmitted once.

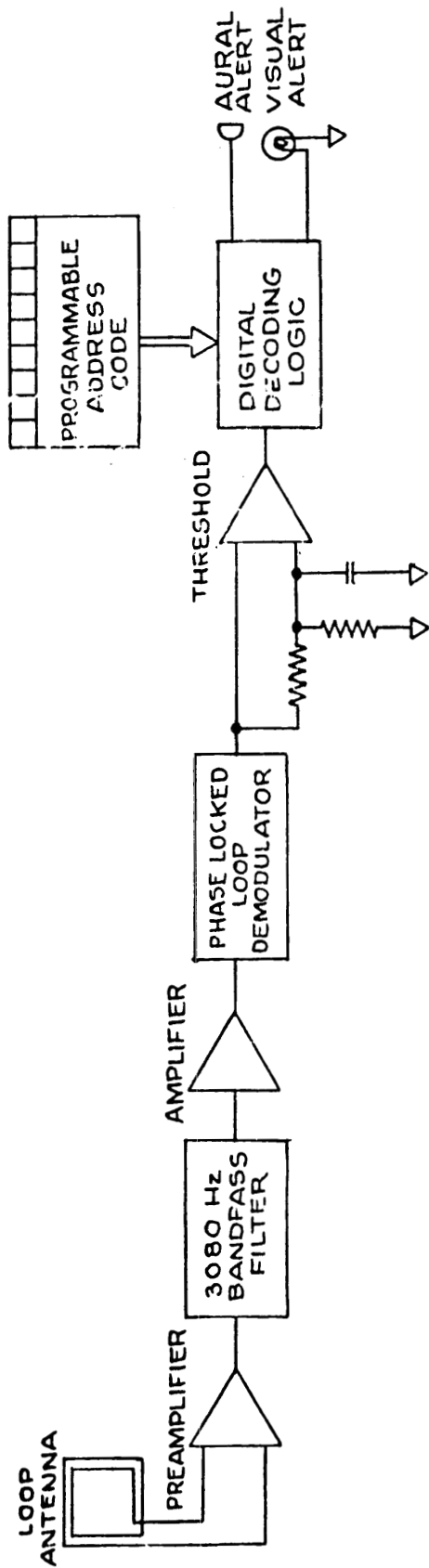
We consider the programmable processor approach to be beyond the scope of the present Call Alert contract. We do feel, however, that the second approach offers a reasonable alternative since it simplifies the hardware interface, lowering production costs without incumbering page processing from the dispatcher's viewpoint. With the above discussion as background, block diagrams for the transmitter and receiver were developed and are illustrated in Figure 10 and 11, respectively. A detailed functional description of the Call Alert System is included as the introduction to the Technical Description below.





CALL ALERT TRANSMITTER

Figure 10



BLOCK DIAGRAM  
CALL ALERT RECEIVER

FIGURE 11

## B. TECHNICAL DESCRIPTION

### 1. Call Alert Transmitter

#### a. Introduction

The call alert transmitter is a self-contained unit, housed in a water tight steel enclosure with dimensions of approximately 8" wide by 10" high by 4" deep, exclusive of the carrying handle and mounting bracket. Connector J1 is located to the left of the front panel and interconnects with a visual display's accessory connector via a four foot cable provided with the transmitter. Loop antenna connector J2 is located to the right of the front panel and contains two spring loaded contacts designed to accept stranded or solid wire to #10 gauge.

The transmitter's control switch panel and 4.5 A-H rechargeable gel-cell battery can be readily accessed by removal of the two screws that retain the hinged front panel. The following switches are located on the panel directly above the transmitter's battery:

- Remote/Local Switch
- Code Select Switches (5)
- Antenna Tuning Switches (5)

A fuse holder is also mounted to the switch panel and will accept a 6 amp 3AG fuse.

If the Rem/Loc Switch is placed in the remote position, the transmitter will accept and process pages received from a visual pager. When a valid code is received, the transmitter will continuously cycle the page code for N periods, where N is equal to the setting of the transmit cycles switch located on the wire wrap card just above the switch panel. This switch may be screwdriver adjusted to transmit from one to nine continuously repeated pages. Since a complete page is transmitted in 530 ms, a sequence of nine repeated pages will require approximately 4.8 seconds to process. This processing time is important to the dispatcher and should be considered by him as pages are posted. If the dispatcher posts a second page before the transmitter has completed a code cycle, the second page will be ignored by the transmitter.

The rechargeable battery housed within the transmitter's enclosure will power the unit for approximately 7,000 pages, provided each page code is transmitted only once. Typically, a page will be repeated several times. As an example, if the transmit cycles switch is set to 5, the battery will be depleted following 1,440 post-page sequences. At a rate of 30 postings per day, and with the transmit cycles switch set to 5, the battery should be recharged at intervals of 1-1/2 months.

The transmitter may be operated independently of the dispatcher's console and the visual display for test purposes. If the Rem/Loc switch is placed in the local position, the transmitter will continuously repeat the page code programmed by the Code Select switches located on the switch panel. Caution is advised when operating the transmitter in the local mode, since a fully charged battery will be depleted in about one hour if the antenna is tuned to resonance.

The correspondence between the page keys of the dispatcher's console, transmitter code and receiver code is indicated in Table 1. The transmitter code is not directly equivalent to the receiver code because the system employs differential phase shift coding. The transmitter code is easily mapped into the receiver code if it is recognized that a change from the previous bit transmitted is interpreted as a logic zero by the receiver. If the current bit being transmitted is the same as the previous bit, regardless if the bit is a one or zero, the receiver processes the bit as a logic one.

The call alert system is designed for a capacity of 32 discrete page codes. Since the dispatcher's console is designed for a maximum of 15 visual pages, slightly less than half the capacity of the call alert system is utilized. During remote operation, the fifth data bit is always transmitted as a logic one. However, during the "local" mode, this bit may be manually programmed by the fifth Code Select Switch.

Antenna tuning switches are located on the switch panel and are used to optimize performance of the transmitter at installation. Power transfer to the loop is at maximum when the antenna is operated at

CALL ALERT SYSTEM CODES

Visual Symbol	Display Code	Transmitter Code			Receiver Code			Receiver S.N. #
		Start	Program	Parity, Stop	Start	Program	Parity, Stop	
	<u>1 2 4 8</u>		<u>1 2 3 4 5</u>			<u>1 2 3 4 5</u>		
①	0 0 0 0	0	0 0 0 0 1	1 1	0	1 1 1 1 0	1 1	
②	1 0 0 0	0	1 0 0 0 1	1 1	0	0 0 1 1 0	1 1	
③	0 1 0 0	0	0 1 0 0 1	1 1	0	1 0 0 1 0	1 1	0 1
④	1 1 0 0	0	1 1 0 0 1	1 1	0	0 1 0 1 0	1 1	0 5
⑤	0 0 1 0	0	0 0 1 0 1	1 1	0	1 1 0 0 0	1 1	
⑥	1 0 1 0	0	1 0 1 0 1	1 1	0	0 0 0 0 0	1 1	
⑦	0 1 1 0	0	0 1 1 0 1	1 1	0	1 0 1 0 0	1 1	0 2
⑧	1 1 1 0	0	1 1 1 0 1	1 1	0	0 1 1 0 0	1 1	0 4
A	0 0 0 1	0	0 0 0 1 1	1 1	0	1 1 1 0 1	1 1	
B	1 0 0 1	0	1 0 0 1 1	1 1	0	0 0 1 0 1	1 1	
C	0 1 0 1	0	0 1 0 1 1	1 1	0	1 0 0 0 1	1 1	0 3
D	1 1 0 1	0	1 1 0 1 1	1 1	0	0 1 0 0 1	1 1	
H	1 0 1 1	0	1 0 1 1 1	1 1	0	0 0 0 1 1	1 1	
J	0 1 1 1	0	0 1 1 1 1	1 1	0	1 0 1 1 1	1 1	
K	1 1 1 1	0	1 1 1 1 1	1 1	0	0 1 1 1 1	1 1	

TABLE 1

resonance. This may best be observed by monitoring the current waveform during the tuning procedure with a portable battery operated oscilloscope. Connect the scope ground to terminal 2 of J2 and the probe a few inches away from terminal 2, toward the loop. This loop connection will function as a current shunt and provides a convenient method of observing antenna current. The loop may be tuned by first switching the transmitter to the local mode. The current waveform is then observed while the antenna tuning switches are operated until the current switching transitions occur at the zero crossing of the current waveform. The current switching transitions will be visible as distinct, fast rising or falling steps and should be adjusted to coincide with the oscilloscope's baseline. The switch bank is designed to accommodate an antenna inductance between 75 and 300  $\mu$ h.

#### b. Nomenclature

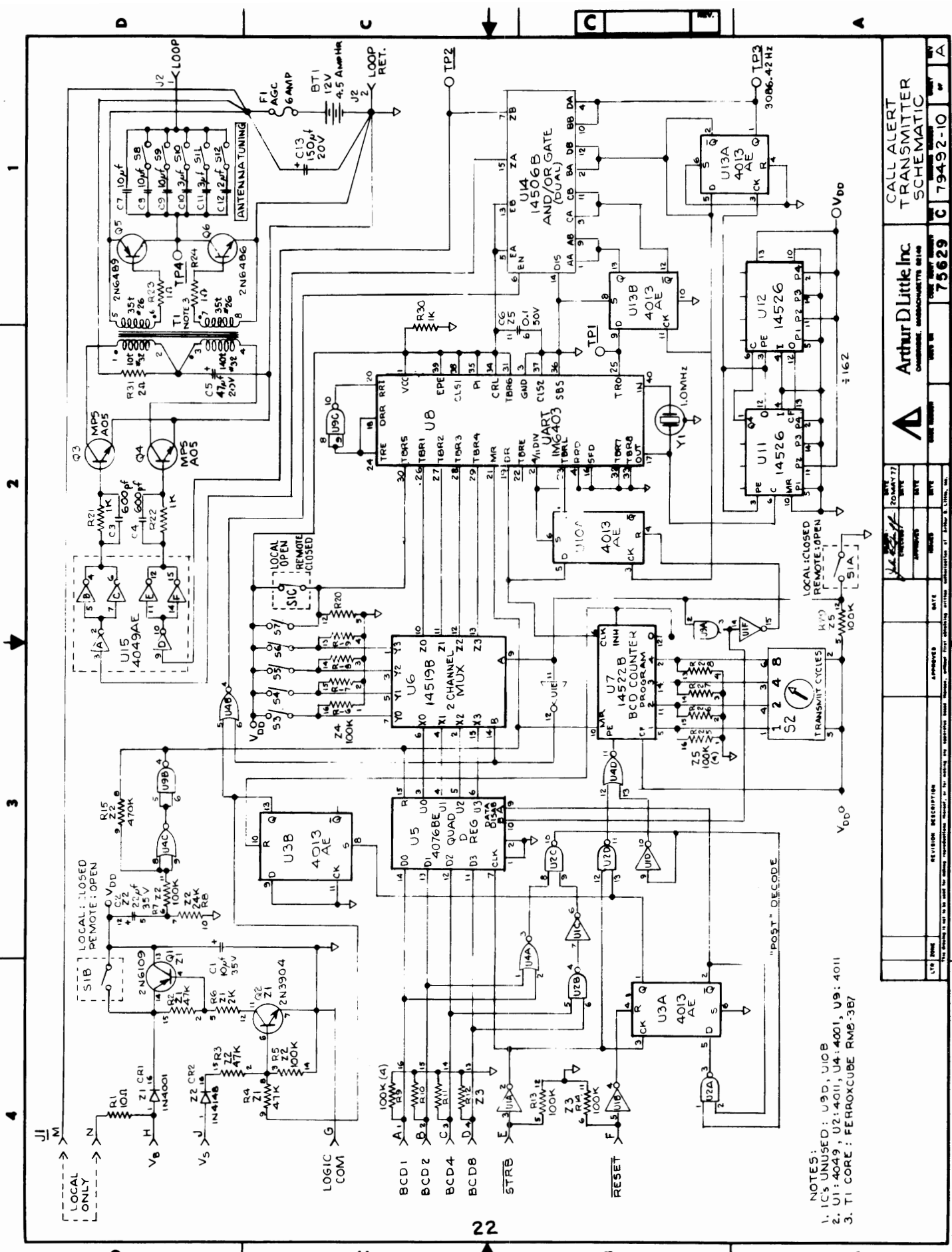
The transmitter schematic is shown in Figure 12. All components are mounted to a wire wrapped board assembly with the exception of the connectors J1, J2 and the battery. Integrated circuits are identified by a U followed by a one or two digit number. Wire wrap sockets are identified at the top of the socket with their appropriate U designation. Most discrete components are mounted on dip headers which are designated with a Z followed by a single digit number. The power output transistors are mounted to a rear plate but are wired directly to the card assembly. The switch panel is wired directly to the card and contains all switches indicated on the schematic with the exception of the Transmit Cycles switch which is plugged into a dip socket, directly on the card.

#### c. Power Supply

During remote operation, 12 vdc is available continuously at J1-H (VB) from a visual display system, Figure 21 J4-H (VB).† As the display powers up in response to d.c. applied to the pager phone line, VS swings positive and the 2N3904 switches on. The 2N6109 conducts and applies 11.5 volts to VDD, the logic supply. Since the current drain is less than 20 ma, the visual pager's battery is not excessively loaded.

---

†Appendix III.



NOTES:  
 1. ICs UNUSED: U9D, U10B  
 2. U1: 4049, U2: 4011, U4: 4001, U9: 4011  
 3. T1 CORE: FERROXCUBE RMB-3B7

REV	DATE	APPROVED	REVISION DESCRIPTION
1	20-MAR-77		
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3			
4			

APPROVED: \_\_\_\_\_ DATE: \_\_\_\_\_  
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 UTR TESTED: \_\_\_\_\_

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CALL ALERT TRANSMITTER SCHEMATIC  
 1

The 2.2 uf capacitor (Z2) is initially discharged and U9B pin 4, the master reset line, is high. The Schmidt trigger formed by U4C and U9B creates a power up reset pulse about 50 ms long. U9 pin 4 switches low at the end of this period, resetting U5, U7 and U8.

d. Visual Pager Interface

The visual pager interface clocks data from Figure 21, J4† appearing on J1 connector pins BCD1 to BCD8 into a storage register (U5) following a valid post code. Gates U2B and U4A monitor the 4 bit bus for a post command (0011). If a post word is detected, the D input to D-flop U3A goes high and the following strobe pulse on J1-E clocks U3A. As the Q output of U3A switches state, the set input of U3B goes high, setting the Q output of U3B.

The reset input of U3B also remains high until jam input counter U7 is preset. If a second strobe does not follow the initial post strobe, then U3B will reset when U3A is reset. This occurs when the visual pager returns to its power down quiescent mode. However, if a second strobe pulse occurs while a post command is stored in U3A, then counter U7 is preset and U3B remains set. The Q output remains high and sources sufficient base current to the 2N3904 to keep this transistor conducting.

Based on the previous discussion, it should be clear that the transmitter remains powered up even though a visual display has shut down, provided the transmitter receives a post command followed by a second data strobe.

Post flop U3A enables the input to quad latch U5, permitting the second data strobe to clock data present on the bus into U5.

e. Transmitter Logic

If S1A is switched to the remote position, data present at the output terminals of the quad latch (U5) is passed through the 2 channel multiplexer U6 to the Z output bus. The multiplexer's parallel output is terminated at the Universal Asynchronous Receiver/Transmitter (UART) transmitter inputs TBRL-4. The UART pin assignments and a brief description of the function of each pin is included in Table 2.

---

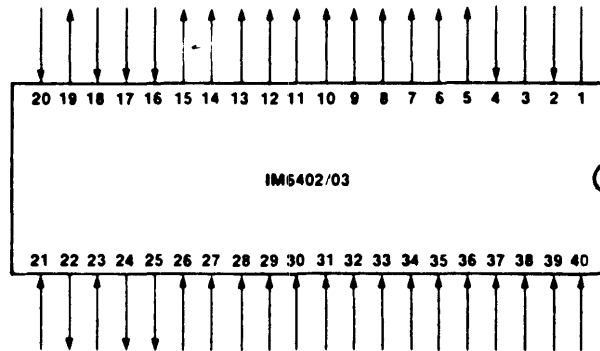
†Appendix III.



## PIN ASSIGNMENT AND FUNCTIONS

PIN	SYMBOL	DESCRIPTION
1	VCC	+5 Volts Supply
2	IM6402-N C IM6403-Control	No Connection 4 11 Stage Divider High 4 Stage Low 11 Stage
3	GND	Ground
4	RRD	A High level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8

PIN	SYMBOL	DESCRIPTION
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	IM6402-RRC IM6403-OSCIN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.



PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE 6	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1-TBR8	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.

PIN	SYMBOL	DESCRIPTION
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-OSCOU	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

Source: INTERSIL, INC., 10900 N. TANTAU AVE., CUPERTINO, CA 95014

Table 2

When jam input down counter U7 is preset by a data strobe, the "0" output, pin 12, switches low, releasing the reset from D-flop U10A. The next low to high 3KHZ clock transition sets the Q output of U10A. The Q transition causes the UART to load its transmitter buffer register from parallel inputs TBRL-5. Two clock cycles later, the UART begins serially transmitting the data, including start, stop and parity bits at TRO (pin 25). The eight bit word begins with a logic low (start bit) and always ends with a logic high, two bits long, characteristic of the parity and stop bits.

The transmitter flags the end of a transmission by raising TRE (pin 24) high. This output is simply inverted and passed on to the Receiver Ready Input (RRI, pin 20). The receiver section of the UART is used to generate a one word delay before the next transmission. This delay allows receivers to resynchronize if they pass through a dead spot or are located in a low signal level area. At the end of a receive cycle, data ready output (DR, pin 19) switches high and counter U7 is clocked. D-flop U10A clocks TBRL (pin 23) and the transmit cycle is repeated until U7 is finally clocked to zero. The actual number of cycles iterated is set by Transmit Cycles switch S2 and may be set from one to nine.

#### f. Modulator

A 3kHz clock (3086.42Hz) is generated by counting down from 1 MHz crystal oscillator that is also used as the master clock for the UART. Programmable binary counters U11 and U12 divide the 1 MHz clock by 162 and U13A divides 617.84 Hz by two to generate the 3086 Hz carrier frequency.

D-flop U13B and And/Or gate U14 together form the phase shift keyed modulator. Two phases of the clock, 180° out of phase are present at the Q and  $\bar{Q}$  outputs of U13A. Either the Q and  $\bar{Q}$  clocks are selected by the complex gate and appear at ZA or ZB as a function of the state of U13B. This D-flop clocks the serial data appearing at TRO synchronously with the 3kHz clock and therefore controls the phase of the clock gated to U14 outputs ZA and ZB.

g. Transmitter Power Output Stage

Complex gate U14 is disabled until a post command is strobed into D-flop U3A and U3B is set. While U14 is disabled, outputs ZA and ZB are low and both MPSA05 driver transistors remain off, conserving power until a post command is detected. When U14 is enabled, the transmitter is keyed as buffer U15 A and D receive the carrier 180° out of phase with respect to each other. Parallel connected inverters U15 B-F provide adequate current gain to drive the two MPS-A05 switching transistors. Transformer T1 provides current gain and level translation to the complementary output stage. The transformer also minimizes power consumption during the quiescent power off mode. The collector current of the driver transistors is approximately 200ma and the base current to the complementary pair is one ampere. The driver and output stages are both sourced from the internal 12-volt battery. The collectors of the complementary pair drive a switchable set of polystyrene capacitors to series tune the loop antenna as described earlier in the introduction. The transmitter's output may be open or short circuited without a danger of destroying components in the output stage. The output transistors will dissipate about 10 watts each when the output is shorted, however, they are mounted to the rear plate to maintain an adequate junction temperature safety margin, even if the ambient temperature reaches 60°C.

h. Local Operation

The transmitter will repeat the code programmed by the Code Select Switches endlessly if Rem/Local Switch S1 is placed in the local position. In this mode, S1A disables the cycle counter U7, S1B bypasses the power up circuit and S1C permits the fifth data bit to be selected. S1A also switches the multiplexer to select data from the code select switches.

## 2. Call Alert Receiver

### a. Introduction

The call alert receiver is a 3 kHz phase shift keying (PSK) receiver of the tuned radio frequency (TRF) type. The receiver is preprogrammed with a set of internal switches to respond to its unique 5 bit digital code by activating an aural and visual alert. Contained within the receiver housing are the rechargeable nickel cadmium batteries and the ferrite loop antenna. The unit is designed for belt or pocket mounting on the person and no external connections are required for normal use. Recharging is accomplished by two external battery terminals located on the bottom of the unit and are current limited for intrinsic safety against shorting.

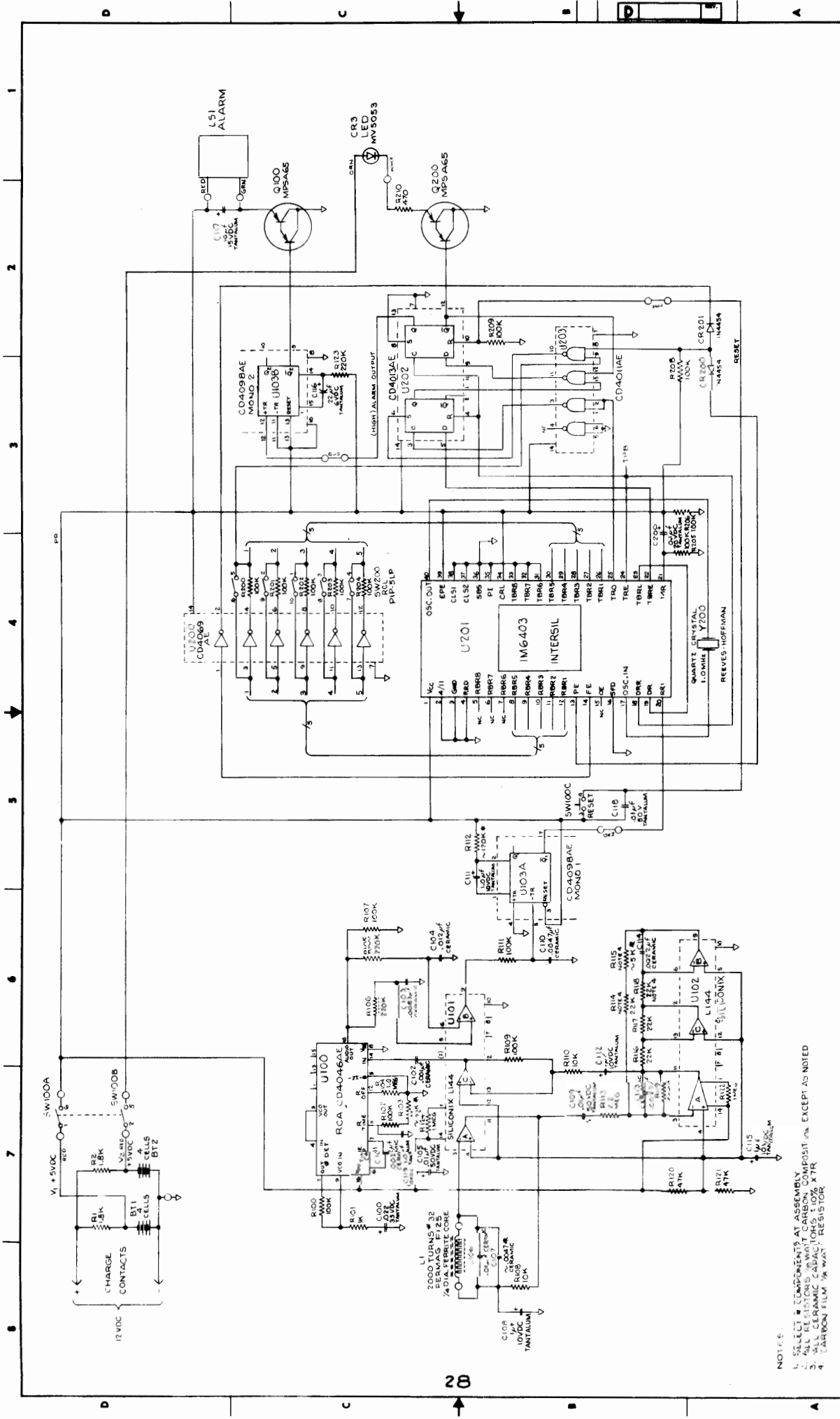
### b. Nomenclature

The receiver schematic diagram is attached as Figure 13. The construction of the unit is such that the components are spread between two double sided printed circuit boards and the case. Components mounted to the case are suffixed with digits 1 to 99 (e.g. C12), components mounted to PC Board #1 are suffixed with digits 100 to 199 (e.g. R104), components mounted to PC Board #2 are suffixed with digits 200 to 299 (e.g. Q204).

Figure 14 depicts the overall assembly of the receiver, including placement of the battery strings. Printed circuit card assembly, fabrication and artwork drawings are included in Figures 15 through 17 for board number one and Figures 18 through 20 for board number two.

### c. Power Supply

All circuits in the receiver are operated from 5 vdc. This voltage is supplied from BT1 and BT2 as follows: BT1 feeds all circuits except the LED visual alert, CR3. CR3 is supplied from BT2. This arrangement was chosen to optimize the battery form factor for the case used; however, it does offer the advantage that if the LED is left on and BT2 is permitted to run down the receiver will still function with the aural alert.



CALL ALERT SCHEMATIC

**Arthur D Little Inc.**  
COMMERCIAL MANUFACTURING DIV.

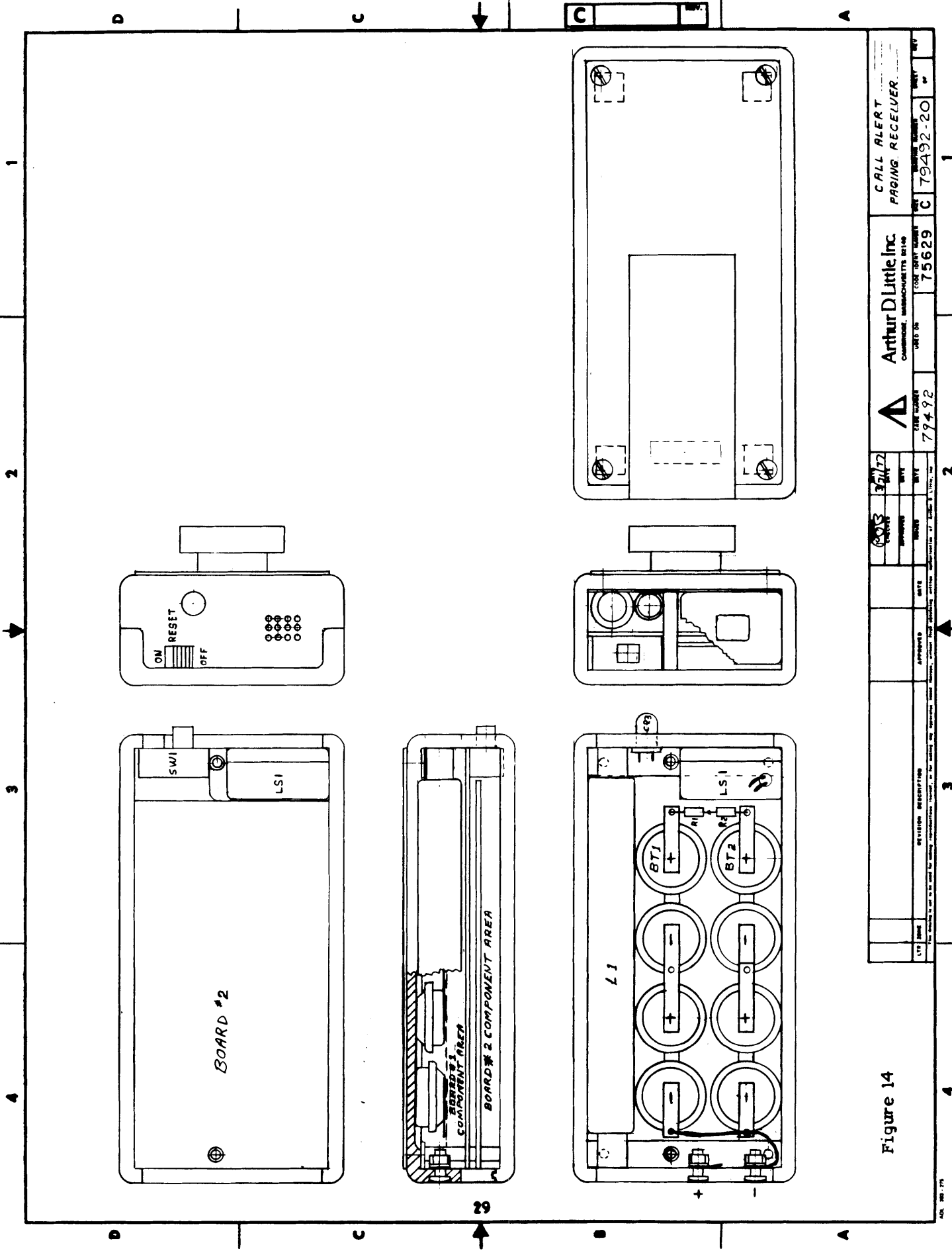
79492-1

79492

REVISION RECORD

NO.	DATE	BY	REASON	APPROVED

NOTES:  
 1. SELECT COMPONENTS AT ASSEMBLY  
 2. ALL RELATIONS WANT CARBON COMPOSIT-ION EXCEPT AS NOTED  
 3. ALL CERAMIC CAPACITORS 10% XTR  
 4. CARBON FILM 1/4 WATT RESISTOR



ARTUR D LITTLE, INC. COMMERCIAL, MASSACHUSETTS 0146		CALL ALERT PAGING RECEIVER	
DATE ORDERED 79492	DATE OF 75629	QUANTITY C	UNIT PRICE 79492-20
REVISED DESCRIPTION	APPROVED	DATE	BY
REV 1			
REV 2			
REV 3			
REV 4			
REV 5			
REV 6			
REV 7			
REV 8			
REV 9			
REV 10			
REV 11			
REV 12			
REV 13			
REV 14			
REV 15			
REV 16			
REV 17			
REV 18			
REV 19			
REV 20			

Figure 14

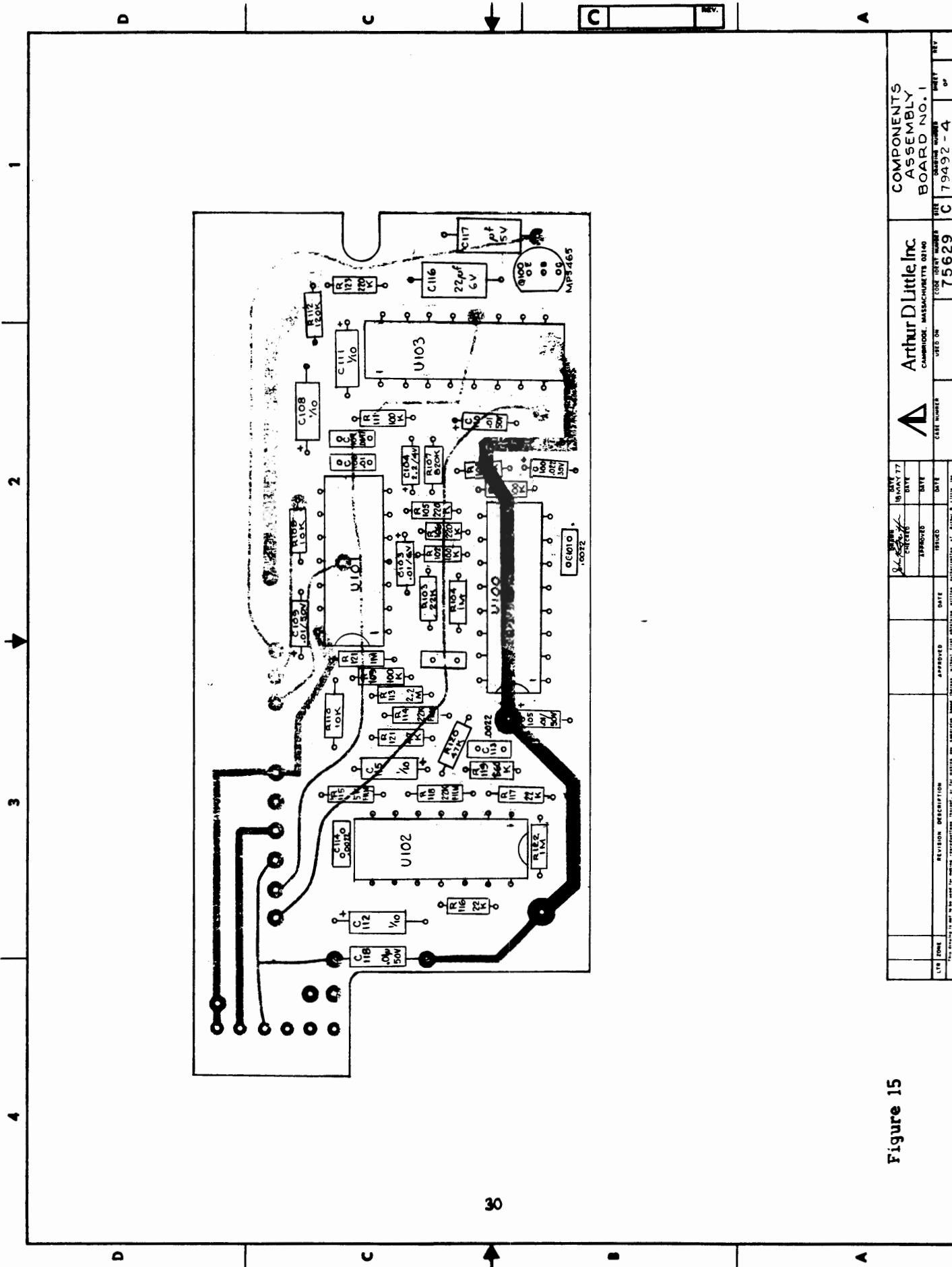


Figure 15

LTV ENGINE		REVISION DESCRIPTION		APPROVED	DATE	ISSUED	DATE	ISSUED	DATE	ISSUED	DATE	ISSUED	DATE

DATE	18 MAY 77
DATE	
DATE	
DATE	

ARTUR D LITTLE, INC.	ARTUR D LITTLE, INC.
CAMBRIDGE, MASSACHUSETTS 02140	CAMBRIDGE, MASSACHUSETTS 02140
USED ON	USED ON
C 75629	C 75629
75629	75629
75629	75629
75629	75629

COMPONENTS ASSEMBLY BOARD NO. 1	
DESIGN NUMBER	C 79492-4
REV	1

4      3      2      1

NOTES 1

1. SCALE 4:1
2. MATERIAL: 1/32 THICK, DOUBLE SIDED, 1 OZ COPPER NEMA TYPE G10 EPOXY BOARD
3. HOLE DRILLING: ALL HOLES .025 ±.003 DIA. AFTER PLATING
4. PLATE: ELECTRODELESS SOLDER (QQ-S-571 SN60)
5. FRONT TO BACK REGISTRATION ±.005
6. DIMENSIONAL TOLERANCES ±.005

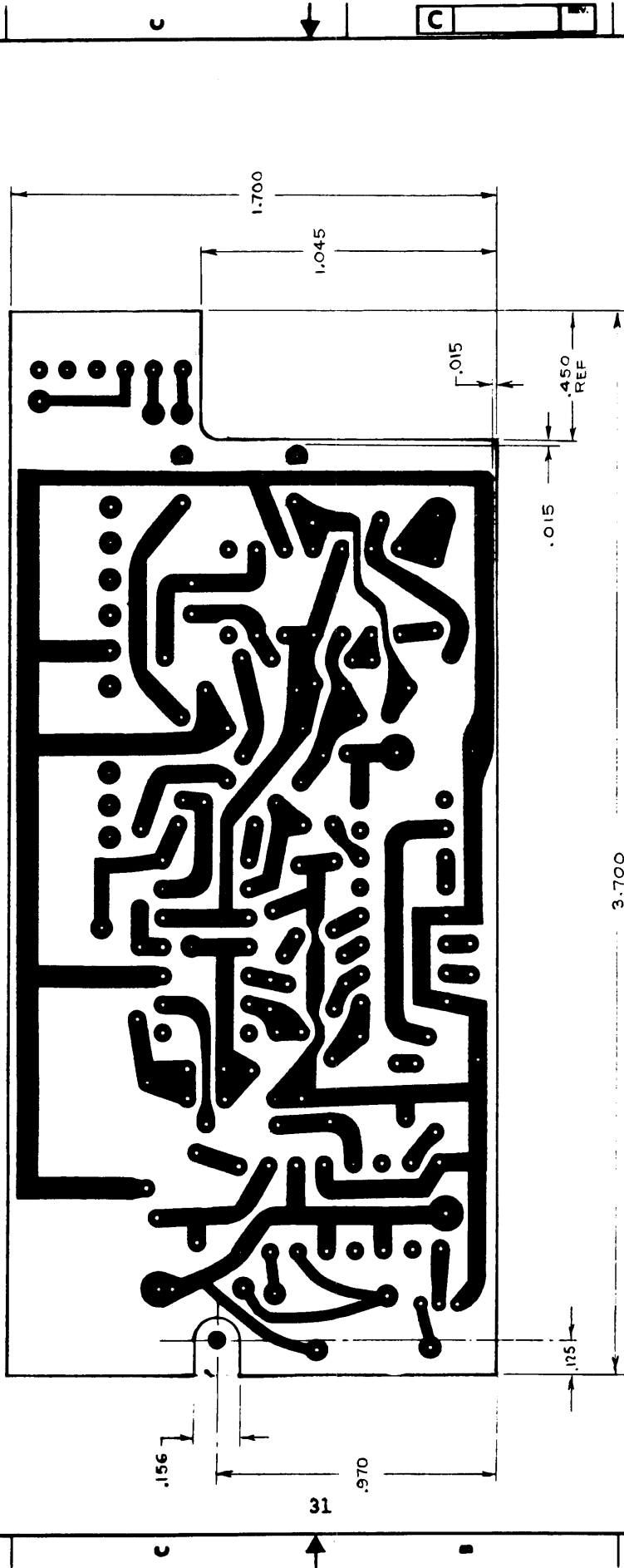
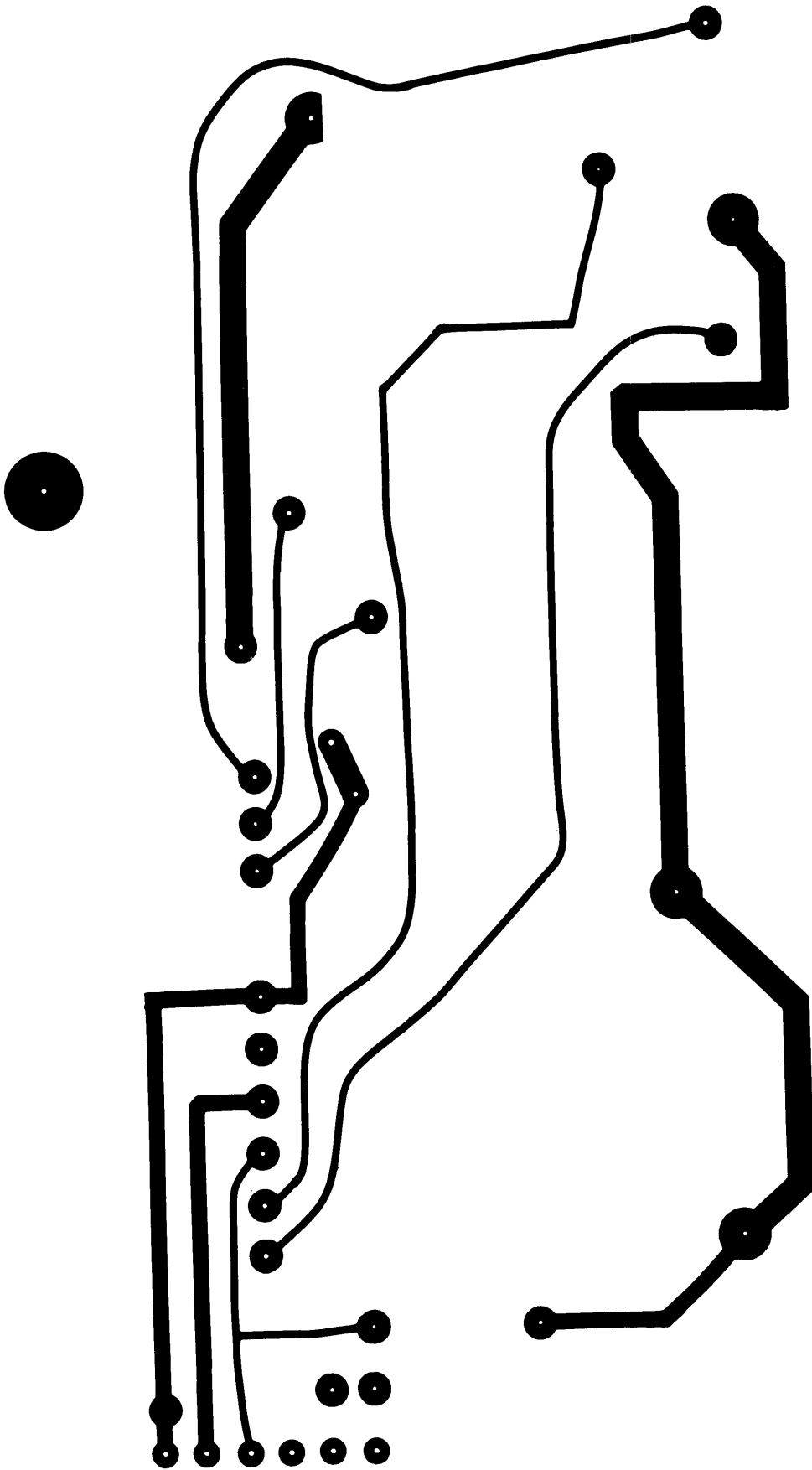


Figure 16

<p>CALL ALERT RECEIVER BOARD NO. 1</p>			
<p>Arthur D Little Inc. CAMBRIDGE, MASSACHUSETTS 02140</p>			
<p>DATE: 10/27/77</p> <p>BY: [Signature]</p>		<p>DATE: 10/27/77</p>	
<p>CHECKED: [Signature]</p>		<p>DATE: [ ]</p>	
<p>APPROVED: [Signature]</p>		<p>DATE: [ ]</p>	
<p>LYR JONE</p>	<p>REVISION DESCRIPTION</p>	<p>APPROVED</p>	<p>DATE</p>
<p>ALL DIMS. UNLESS OTHERWISE SPECIFIED ARE IN MILLIMETERS</p>			
<p>CASE NUMBER</p>	<p>CODE</p>	<p>PROJECT NUMBER</p>	<p>DATE</p>
<p>C 79492 - 3</p>	<p>75629</p>	<p>C 79492 - 3</p>	<p>1977</p>





COMPONENT SIDE  
REDUCTION 4:1

CALL ALERT RECEIVER  
BOARD NO. 1  
ARTWORK MASTER  
DRAWING NUMBER 79492-2  
SHEET 1 OF 2

Figure 17A

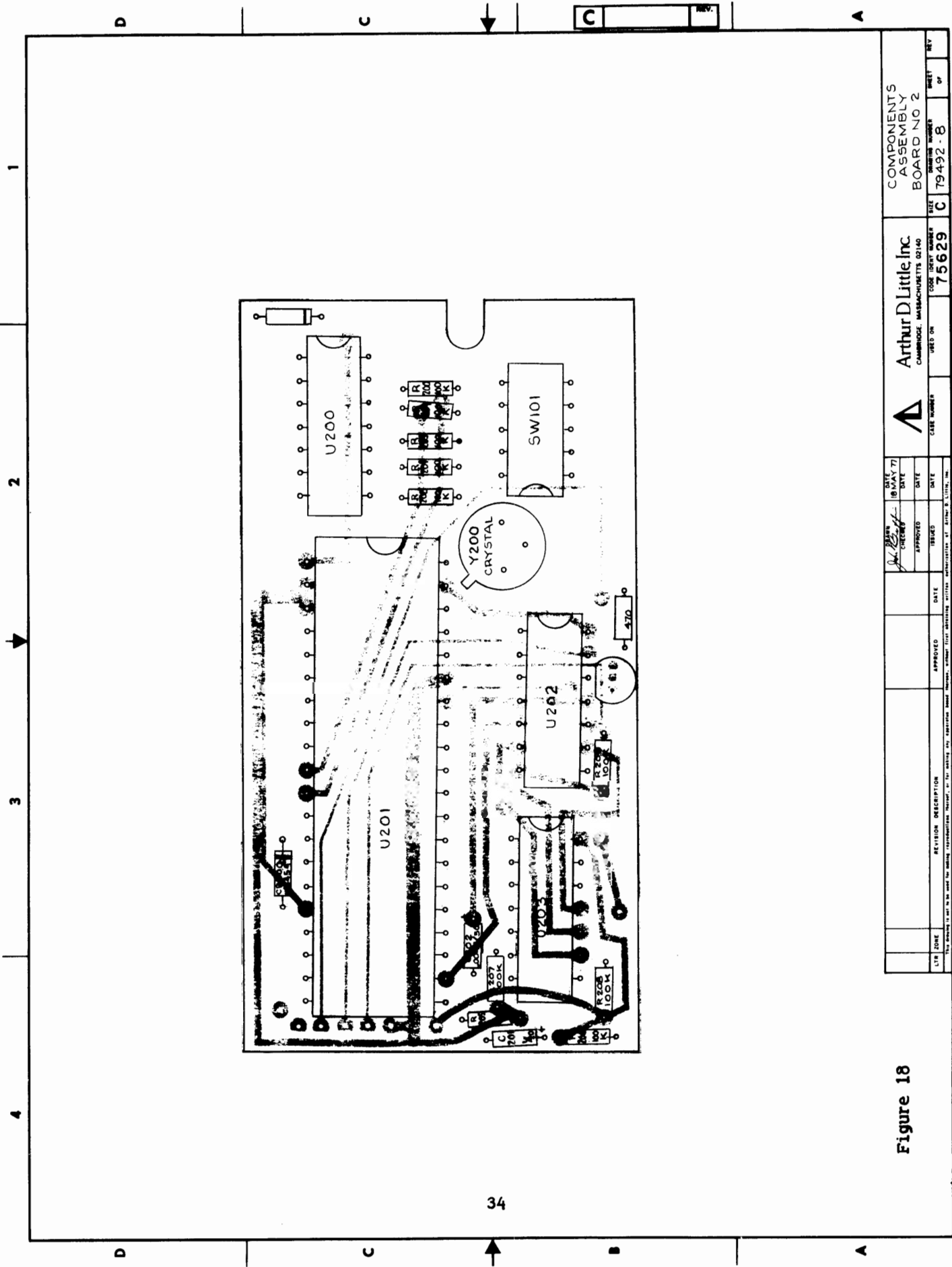

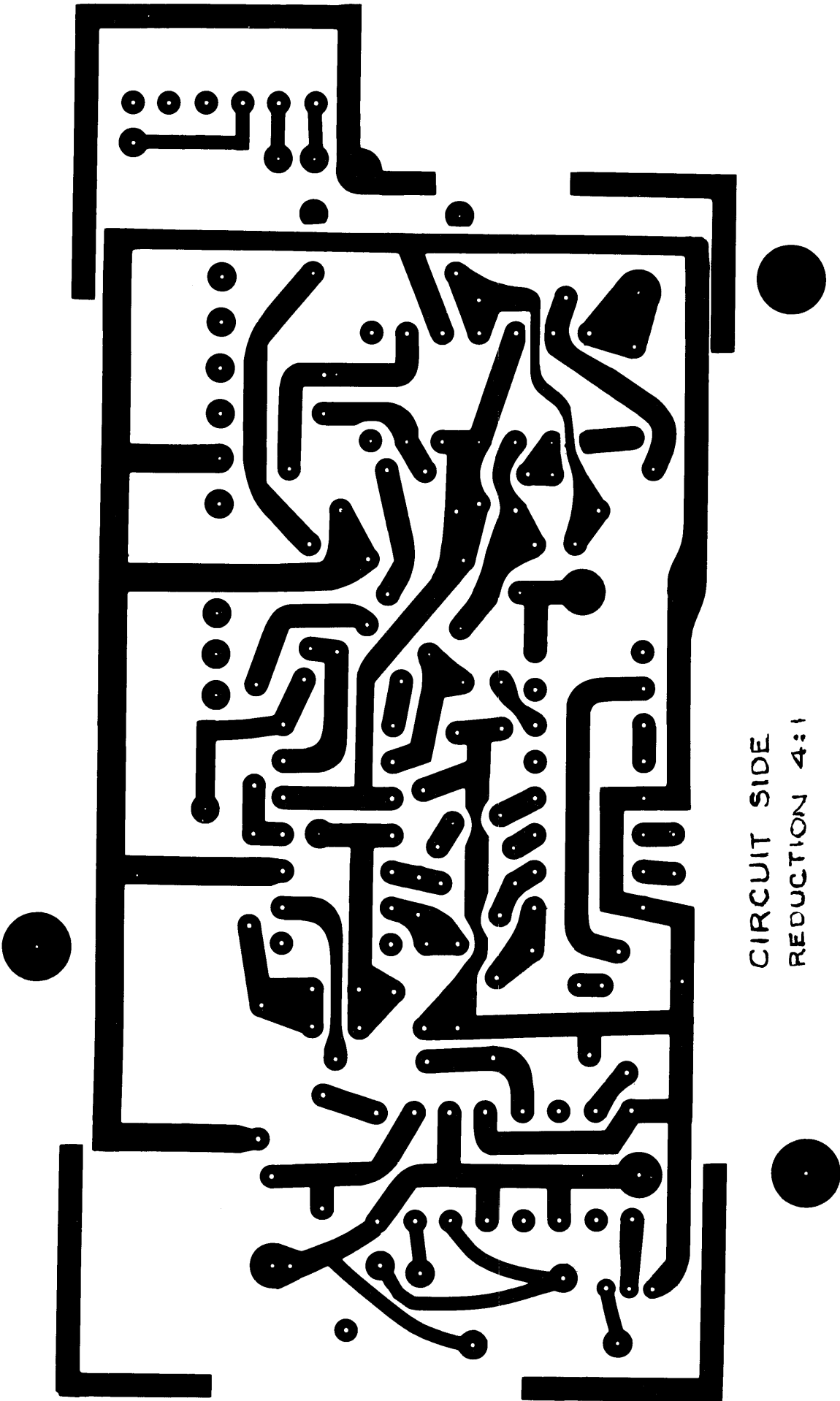


Figure 18

LTZ ZONE	REVISION	DESCRIPTION	APPROVED	DATE	ISSUES	DATE	ISSUES	DATE	ISSUES	DATE	ISSUES


**Arthur D Little, Inc.**  
 CAMBRIDGE, MASSACHUSETTS 02140  
 CODE IDENT NUMBER **75629**  
 FILE NUMBER **C 79492-8**

FILE	ISSUES NUMBER	SHEET	REV
<b>C</b>	<b>79492-8</b>	<b>1</b>	<b>1</b>



CIRCUIT SIDE  
REDUCTION 4:1

CALL ALERT RECEIVER  
BOARD NO. 1  
ARTWORK MASTER  
DRAWING NUMBER 79492-2  
SHEET 2 OF 2

Figure 17B

NOTES:

1. SCALE: 4:1
2. MATERIAL:  $\frac{1}{32}$  THICK, DOUBLE SIDED, 1 OZ COPPER  
NEMA TYPE G10 EPOXY BOARD
3. HOLE DRILLING - EXCEPT AS DIMENSIONED  
ALL HOLES .025  $\pm$  .003 AFTER PLATING
4. PLATE: ELECTROLESS SOLDER (QQ-S-571 5NGO)
5. FRONT TO BACK REGISTRATION  $\pm$ .005
6. DIMENSIONAL TOLERANCE  $\pm$ .005

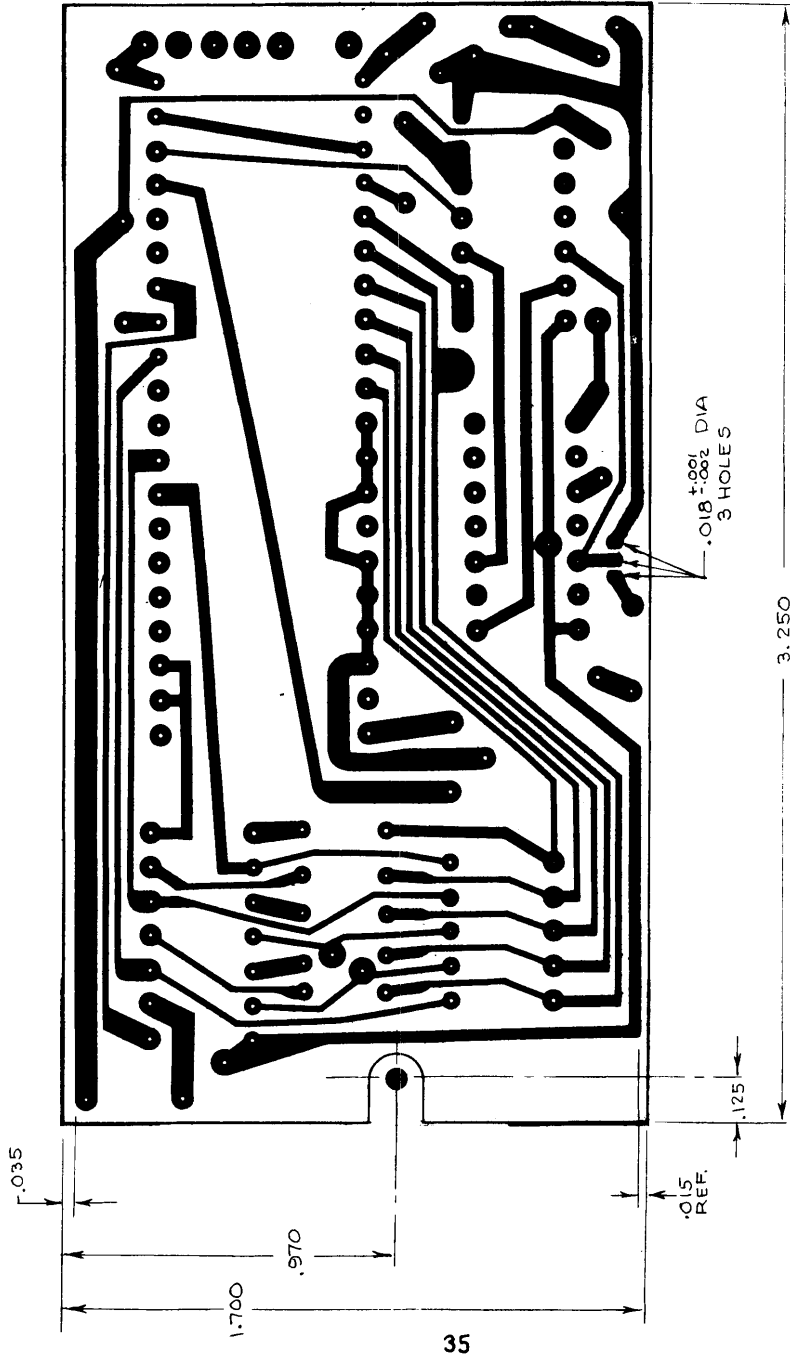


Figure 19

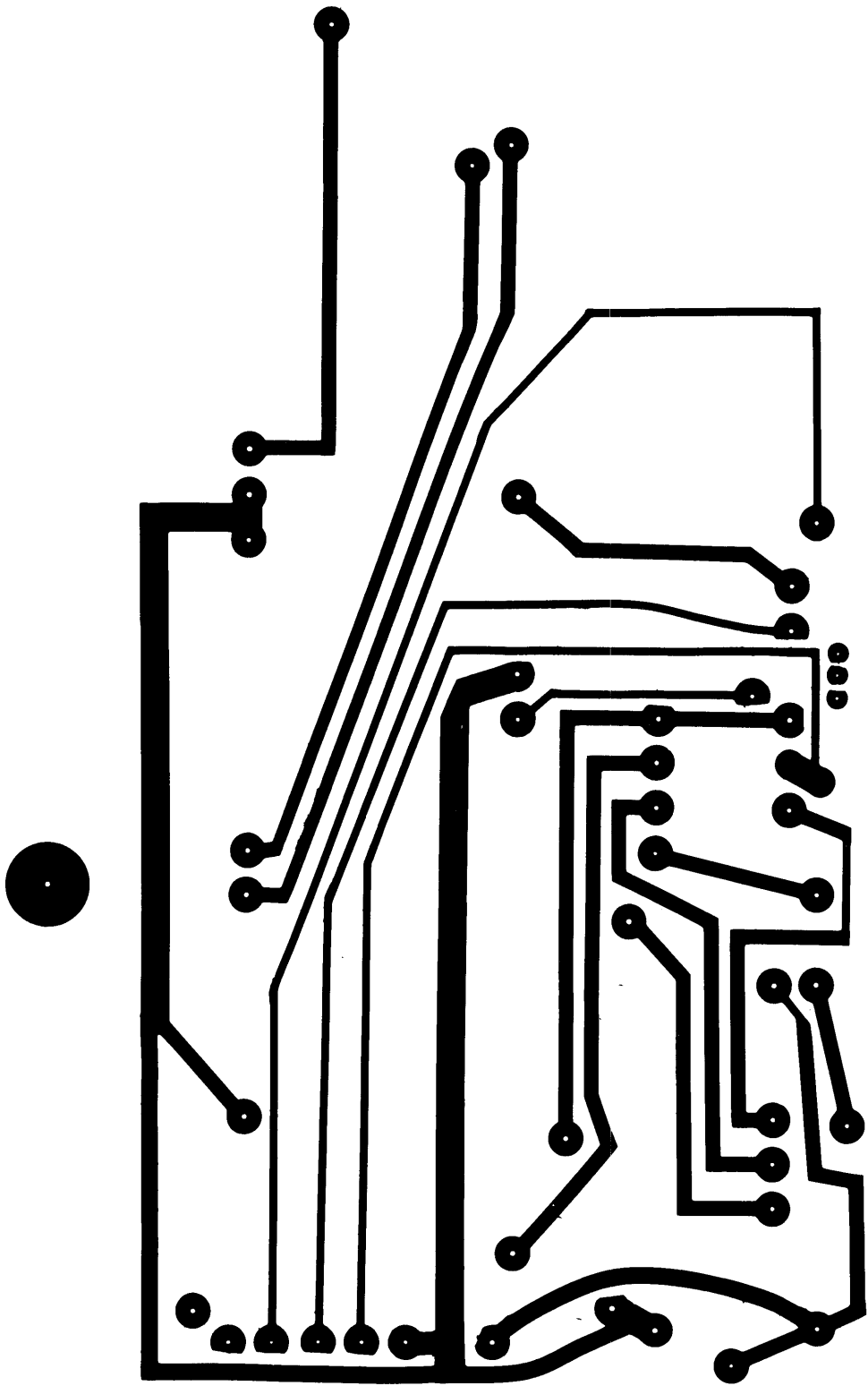
DATE	BY	DATE	BY	DATE	BY
	DESIGNED		APPROVED		
	DRAWN		REVIEWED		

DATE	DESCRIPTION	APPROVED	DATE
	REVISION		

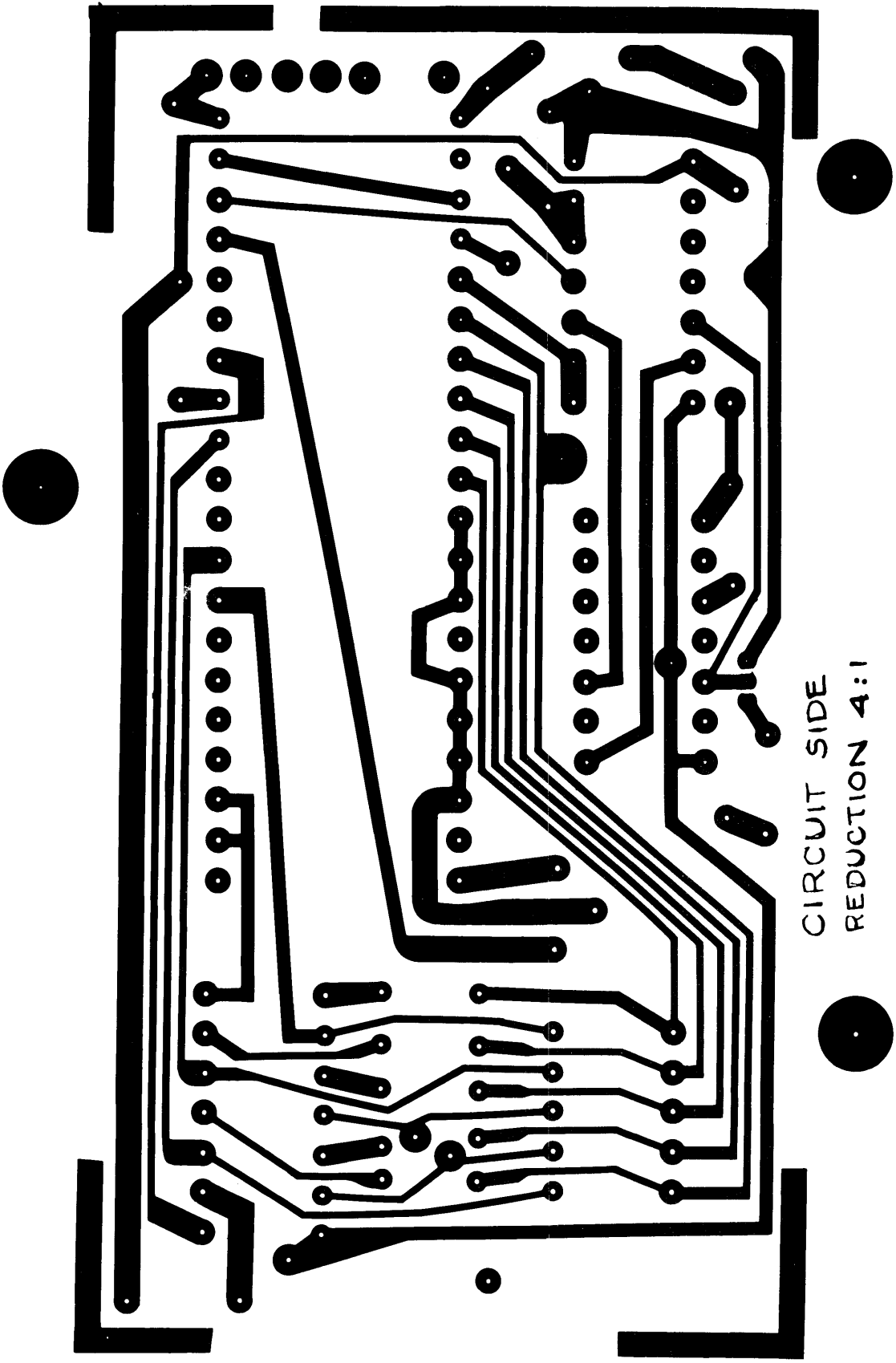
ARTUR D LITTLE INC CAMBRIDGE, MASSACHUSETTS 02140	USED ON	CODE IDENT NUMBER	75629	CASE NUMBER	
CALL ALERT RECEIVER BOARD NO 2	DRAWING NUMBER	C	79492-7	SHEET	1
	REV			OF	



COMPONENT SIDE  
REDUCTION 4:1

CALL ALERT RECEIVER  
BOARD NO. 2  
ARTWORK MASTER  
DRAWING NUMBER 79492-6 SHEET 1 OF 2

Figure 20A



CIRCUIT SIDE  
REDUCTION 4:1

CALL ALERT RECEIVER  
BOARD NO. 2  
ARTWORK MASTER  
DRAWING NUMBER 79492-6  
SHEET 2 OF 2

Figure 20B

Switch SW100 removes all power (both batteries) from the circuit when operated but does not break the circuit to the charging contacts. Charging is accomplished by means of an external charger which applies 12 Vdc to the charging contacts. The internal current limiting resistors R1 and R2 approximate a 10 mA constant current source charger for the batteries. The batteries are rated to withstand this charge rate indefinitely and should be fully recharged after 16 hours.

#### d. Receiver Front End

The receiver front end consists of integrated circuits U101, A & C and U102. This section of the receiver accepts the input signal from the antenna, amplifies and filters it before applying it to the demodulator.

The antenna assembly is a high Q (about 30) parallel resonant LC circuit. The exact resonant frequency is trimmed with the "select at test" capacitor C107. U101 is biased with R121 at 5  $\mu$ A and under these conditions the loop antenna amplifier, U101A, runs with an open loop gain of about 60 dB. The DC quiescent bias point for U101A&B, and all of U102 is set at about half supply by R120 and R121. This bias point is decoupled with C115 to ground. The output of U101A is coupled by DC blocking capacitor C109 to the active bandpass filter circuit of U102.

The active bandpass filter is a three amplifier state variable filter using all three sections of U102. The state variable filter was chosen to provide a Q of 30 while minimizing the sensitivity to component variations over frequency and tolerance. The center frequency of the filter is trimmed by the "select at test" resistor R114. The midband gain of the active filter is limited by the divider input resistor R113 so that the active filter remains in the linear region even when U101A is driven into full clip. This approach insures that noise and strong signals are controlled in the amount of energy that can be coupled in to the demodulator which reduces the probability of falsing on extraneous signals.

The output of the active filter is buffered with a single amplifier

section consisting of U102C with a nominal gain of 20 dB. The output of U101B is coupled to the demodulator through C102.

e. Demodulator

The demodulator circuit consists of U100, U101B and U103A. This circuit functions by demodulating the carrier PSK phase transitions into 5 Vdc controlled pulse width logic level transitions.

U100 is a phase locked loop integrated circuit. The voltage controlled oscillator (VCO) is nominally tuned to the 3 kHz carrier frequency by C101 and R102. This frequency is trimmed at test by selecting R103. R104 insures the oscillator starting under worst case battery conditions. The loop is locked through a proportional plus integral control loop filter consisting of R100, R101, and C100. The filter is selected so that the minimum bandwidth consistent with the 30 bit per second signalling rate is used. The values were selected empirically to set intersymbol interference to zero at the maximum 30 baud signalling rate. The filter damping was set to at least one cycle of ringing to insure that both a positive and negative going transition are available regardless of the direction of phase change. The phase detector output is buffered internally in U100 and is supplied to the audio output pin 10.

The phase locked loop output divides at pin 10 into two separate paths into the comparator, U101B. The first path through R106 is filtered by C103 to remove the 3 kHz carrier. The other path through R105 to C104, provides a longer integration interval compared to R106 and C103. So the average DC level of the phase locked loop appears at pin 6 of U101. When a phase transition occurs in the phase locked loop, the comparator U101 translates the 50 mV loop output into a 5 VDC pulse. The comparator output at pin 9 of U101 is further filtered to reduce the 3 kHz carrier by R111 and C110 and applied to the monostable U103A.

The negative going transition appearing at pin 5 of U103A triggers the monostable. The timing interval is set by the RC product of R112 and



C111. The timing is adjusted to be equal to one nominal bit interval at the 30 baud rate. The monostable is further configured to be re-triggerable to any phase changes that occur in the carrier before it resets. In the quiescent state the monostable output at pin 7 of U103A is high.

#### f. Decoder

The decoder circuit consists of U201, U200, U203, U202, and U103B. The decoder functions by accepting the serial bit stream from the demodulator and provides an alarm signal to the interface circuitry if the received code sequence matches the preprogrammed pager code.

The following conventions will be assumed for coding: A phase transition in the transmitted signal causes a "0" to be input to the decoder, no transition causes a "1" to be input. The bit intervals are equally spaced for all bits. The code format consists of a single start bit of a "0" followed by the five data bits, followed by a single parity bit, ended by a single stop bit of a "1". The code is entered into the pager using SW200 where a switch closure is a "1" and an open is a "0". The code will be stated as bit position 1 through 5 as noted on U200 from left to right.

For additional reference, a listing of the pins and functions of U201 is indicated in Table 2.

The serial bit stream from pin 7 of U103 is input to the Universal Asynchronous Receiver Transmitter (UART) U201 into the receiver input, pin 20. The UART timing is controlled by quartz crystal Y200 and the divider strapping on pin 2 of U201. The UART separates the serial bit stream into the five parallel code bits and makes them available on pins 12 through 8 as noted on the schematic. In addition, parity and framing error outputs are made available on pins 12 and 14 respectively. A data ready strobe is provided on pin 19 which is reset by input to pin 18. The receiver outputs are not reset by pin 18, only the strobe is reset, so the data and the error outputs remain latched until the next code sequence of 8 bits is received (start, 5 code, one parity, one stop).

The five parallel code bits are routed through the circuitry about U200. This IC and the code select Switch U200 permit selected code bits to be inverted. The programming is such that the correct code will produce all "1"s at the transmitter input to the UART, pins 26 through 30.

The converted code pins from SW200 are loaded into the transmitter section of U201 by the data ready strobe from pin 19 to the load input pin 23. When the code sequence has been serially clocked out of the transmitter at pin 25, the empty output of the transmitter at pin 24 provides a receiver data strobe clear into U201 pin 18.

The remainder of the logic functions as follows: The initial "0" start bit from the pin 25 transmitter output of U201 is ignored by the U202 flip flop because of the pulse delay output from the buffer register empty output pin 22 of U201. If the remainder of the other code and parity pulses output from pin 25 have no high to low transitions U202 will be clocked on through pin 11 and outputs to the alarm interface will be provided. Additional gating from the number one bit position at pin 5 of SW200 is provided into pin 9 of U203 to insure that the decoding only occurs if all the code outputs at SW200 are high (i.e. no low to high transitions plus number one bit high means all are high since the last stop bit is always high). Decoding will be inhibited by a framing or parity error on pins 13 or 14 of U201.

A correct decoding sequence causes the "0" flip flop U202 to latch with pin 13 high and pin 12 low. The pin 12 output is routed to the LED driver Q200 and turns on the LED. The pin 13 output triggers U103B for an approximate 1 second interval determined by C116 and R123. The output of U103B at pin 9 feeds the aural alarm through the driver transistor Q100.

The alarm will sound only once and the LED will remain latched on until U202 is reset by SW100C.

### III. MANUFACTURING COST ESTIMATE

#### A. SUMMARY

The cost estimates for the individual assemblies that comprise the call alert system are attached as Appendix I and are based on our prototype design. Specific features of the prototype will not necessarily find their way into a production system, particularly in view of the test functions built into the transmitter.

The cost estimates in Appendix I are based on the following assumptions:

- The call alert receiver will be manufactured in lots of one hundred units.
- The call alert transmitter will be manufactured in lots of ten units.
- This is factory cost; that is, the cost of materials and direct labor only. The labor costs include overhead for factory space and supervision. We assumed an average of \$12 per hour for all types of direct labor.
- These prices do not include the cost of development, sales or administration. For a low-volume, job-shop type of manufacturing situation, which this is, the factory cost would be marked up 200-300 percent to get the sell, or list price.
- The cost of production engineering and documentation is not reflected in these prices. Complete parts lists and fabrication drawings as well as the design of a printed circuit board for the call alert transmitter will be required before a production run of any size could be started.

#### B. CALL ALERT RECEIVER

Although printed circuit boards were used in the prototype design of this unit and their cost savings are reflected in the cost estimates in Appendix I, further cost reductions are possible by the elimination of custom fabricated parts. For instance, if the extensively modified

commercial enclosure is replaced by a custom designed injection molded enclosure, and the purchased clip assembly is replaced by a custom designed aluminum die casting, then all the costs for fabricated parts would be eliminated. This would reduce the factory cost from approximately \$167 to \$125. If the antenna is produced on a semiautomatic coil winder instead of a laboratory type coil winder, then the factory cost would be reduced another \$9. These construction and labor savings should be instituted before a significant production volume is started.

C. CALL ALERT TRANSMITTER

The transmitter will never be manufactured in as high a volume as the receiver, but it will still be cost effective to change from wire wrap construction to printed circuit wiring. This would eliminate the cost of I.C. sockets and component carriers as well as the labor costs for wire wrapping. The transmitter manufacturing cost would change from approximately \$594 to \$330.

APPENDIX I

COST ESTIMATES

ITEM NO	QTY REQ	PART NUMBER OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SOURCE	REVISION LETTER
1			Enclosure and Panel (including labor to modify)		\$ 25.50
2			Vector Board Assembly Components		142.14
			Labor to Assemble and Test		240.00
3			Switch Panel Assembly Components		31.95
			Labor to Assemble		6.00
4			Battery		22.00
5			Misc. Components		10.79
6			Misc. Fabricated Parts (Includes Labor to Manufacture)		19.50
7			Final Assembly and Test Labor (Including Cable Harness)		96.00
				*Factory Cost, Total	\$593.88

PREPARED BY \_\_\_\_\_ DATE \_\_\_\_\_ APPROVED BY \_\_\_\_\_ DATE \_\_\_\_\_

**Arthur D Little, Inc**  
CAMBRIDGE, MASSACHUSETTS 02140

Cost Estimate for Call Alert Transmitter

TITLE: \_\_\_\_\_

PARTS LIST NUMBER: 79492

**ELECTRONIC SYSTEMS SECTION**

SHEET 1 OF 1


\*If manufactured in lots of 10.



APPENDIX II

PARTS LIST



ITEM NO	QTY REQ	PART NUMBER OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SOURCE	REVISION LETTER
1	1		Stainless Steel Backplate	ADL 79492-23	
2	2		Stainless Steel Brackets	ADL 79492-22	
3	2		Brass Standoffs, Cadmium Plated	ADL 79492-21	
4	1		Cover and Clip Kit Motorola NLN-8279A	Motorola	
5	1		Electronic Box EL-410	Rose Enclosures	
6	8	BT1,2	Batteries B50T	Eveready	
7	2	RI,R2	1.8K Resistors 1/4w 10%	Allen Bradley	
8	1	CR3	LED MV5053	Monsanto	
9	1	L1	Antenna; 1" Long Coil, 2000 Turns #32 Enamel Wire, ADL Centered on 4" Long Permag Rod #F125-1. Lp = 185 mh, Cp = 0.05 uf, Q = 30.		
10	1		LSI - Alarm AI-105	Projects Unlimited	
 <b>Arthur D Little Inc</b> <small>CAMBRIDGE, MASSACHUSETTS 02140</small>			Enclosure Assembly Call Alert Receiver <small>TITLE</small>		REVISION LETTER
<b>PARTS LIST</b>			PARTS LIST NUMBER: 79492		REVISION DATE
					SHEET 1 OF 1

ITEM NO	QTY REQ	PART NUMBER OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SOURCE	
1	4	R100,102,109,111	100K, 1/8w 10%	Allen Bradley	
2	1	R101	1K	↑	
3	1	R103	22K		
4	3	R104,122,124	1 meg.		
5	1	R105	220K		
6	2	R106,123	220K		
7	1	R107	100K		
8	2	R108,110	10K		
9	1	R112	120K		
10	1	R113	2.2 meg.		
11	2	R114,118	22K Carbon Film 1/8w		MEPCO
12	1	R115	5K Carbon Film 1/8w	MEPCO	
13	2	R116,117	22K, 1/8w 10%	Allen Bradley	
14	1	R119	560K "	Allen Bradley	
15	2	R120,121	47K "	Allen Bradley	
16	1	C100	.022uF/35V Tantalum MZP Series	Corning	
17	3	C101,113,114	.0022uF Ceramic UK Series	Centralab	
18	1	C102	.001uF Ceramic UK Series	Centralab	
19	1	C103	0.0083uF Ceramic UK Series	Centralab	
20	1	C104	0.012uF Ceramic UK Series	Centralab	
21	4	C105,109,110,118	0.0047uF Ceramic UK Series	Centralab	
22	2	C106,107	.01uF Ceramic UK Series	Centralab	
23	4	C108,111,112,115	1uF/10V Tantalum MZP Series	Corning	
24	1	C116	22uF/6V Tantalum MZP Series	Corning	
25	1	C117	10uF/15V Tantalum MZP Series	Corning	
PREPARED BY		DATE	APPROVED BY	DATE	REVISION LETTER
ARTHUR D LITTLE INC CAMBRIDGE MASSACHUSETTS 02140					
PARTS LIST			BOARD #1 ASSEMBLY CALL ALERT RECEIVER		TITLE
			PARTS LIST NUMBER: 79492		SHEET 1 OF 2



ITEM NO	QTY REQ	PART NUMBER OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	1/8w	10%	SOURCE
1	10	R200-206, 208-209	100K	1/8w	10%	Allen Bradley
2	1	R210	470 <del>4</del>	"	"	Allen Bradley
3	1	C200	.1 $\mu$ F/20V		Tantalum MZP Type	Corning
4	1	U200	CD4069AE			RCA
5	1	U201	IM6403			Intersil
6	1	U202	CD4013AE			RCA
7	1	U203	CD4011AE			RCA
8	2	CR200, 201	IN4454			Motorola
9	1	Q200	MPSA65			Motorola
10	1	Y200	Crystal, 1.0 MHz, TO-5 Size			Reeves-Hoffman

REVISION LETTER	REVISION DATE	SHEET 1 OF 1
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Board #2 Assembly  
Call Alert Pager

TITLE  
PARTS LIST NUMBER: 79492



Arthur D Little Inc  
CAMBRIDGE, MASSACHUSETTS 02140

ELECTRONIC SYSTEMS SECTION

PREPARED BY \_\_\_\_\_ DATE \_\_\_\_\_ APPROVED BY \_\_\_\_\_ DATE \_\_\_\_\_


**PARTS LIST**

ITEM NO	QTY REQ	PART NUMBER OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SOURCE
1	1	R1	10 $\Omega$ 1/4w 10% Resistor	Allen Bradley
2	3	R2, 3, 4	47K	
3	18	R5, 7, 9-14, 16-20, 25-29	100K	
4	1	R6	2K	
5	1	R8	24K	
6	1	R15	470K	
7	3	R21, 22, 30	1K	
8	2	R23, 24	1 $\Omega$ 1/4w 10%	Allen Bradley
9	1	C1	10uF/35V, TAN., T360 Series Capacitor	Kemet
10	1	C2	22uF/35V, TAN., T360 Series	Kemet
11	2	C3, 4	600pF, MICA, DM15 "	Cornell Dublier
12	1	C5	47uF/20V T360 Series	Kemet
13	1	C6	.1uF/50V UK "	Centralab
14	3	C7, 8, 9	10uF, POLYCARBONATE, X483 Series	TRW
15	2	C10, 11	3uF, POLYCARBONATE, X483 Series	TRW
16	1	C12	2uF, POLYCARBONATE, X483 Series	TRW
17	1	C13	150uF/20V, TAN., T360 Series	Kemet
18	1	Q1	2N6109, PNP Transistor	Motorola
19	1	Q2	2N3904, NPN	G.E.
20	2	Q3, 4	MPSA05, NPN	Motorola
21	1	Q5	2N6489, PNP	R.C.A.
22	1	Q6	2N6486, NPN	R.C.A.
<b>PREPARED BY</b> _____ <b>DATE</b> _____ <b>APPROVED BY</b> _____ <b>DATE</b> _____			<b>Call Alert Transmitter</b>	
<b>ARTHUR D LITTLE INC.</b> <small>CAMBRIDGE, MASSACHUSETTS 02140</small>			<b>REVISION LETTER</b>	
<b>ELECTRONIC SYSTEMS SECTION</b>			<b>REVISION DATE</b>	
<b>PARTS LIST</b>			<b>TITLE</b>	
<b>PARTS LIST</b>			<b>PARTS LIST NUMBER: 79492</b>	
<b>PARTS LIST</b>			<b>SHEET 1 OF 3</b>	

ITEM NO	QTY REQ	PART NUMBER OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SOURCE
23	1	CR1	Diode	TI
23A	1	CR2	"	Fairchild
24	1	U1	IC's	RCA
25	2	U2,9		
26	3	U3,10,13		
27	1	U4		
28	1	U5		
29	1	U6		
30	1	U7		
31	1	U8		
32	2	U11,12		
33	1	U14		
34	18		I.C. Sockets Wire Wrap 703-3898-01-03-16	Cambion
35	1		Vector Board 85624WE	Vector
36	5		I.C. Component Carriers 3728-01-03-00	Cambion
37	1		Enclosure A-10-N8P Hoffman Engineering	ADL 79492-24
38	1		Back Panel 6 1/4 x 8 1/4 Aluminum	ADL 79492-25
39	1		Switch Panel 1 1/2 x 6 1/4 Aluminum	ADL 79492-26
40	1	BT1	Battery 4.5 AH 12V	Globe
41	1	MS3102A-20-20P	Connector Receptacle	Amphenol

REVISION LETTER  
REVISION DATE  
SHEET 2 OF 3

Call Alert Transmitter  
TITLE  
PARTS LIST NUMBER: 79492

 Arthur D Little, Inc.  
CAMBRIDGE, MASSACHUSETTS 02140

**ELECTRONIC SYSTEMS SECTION**

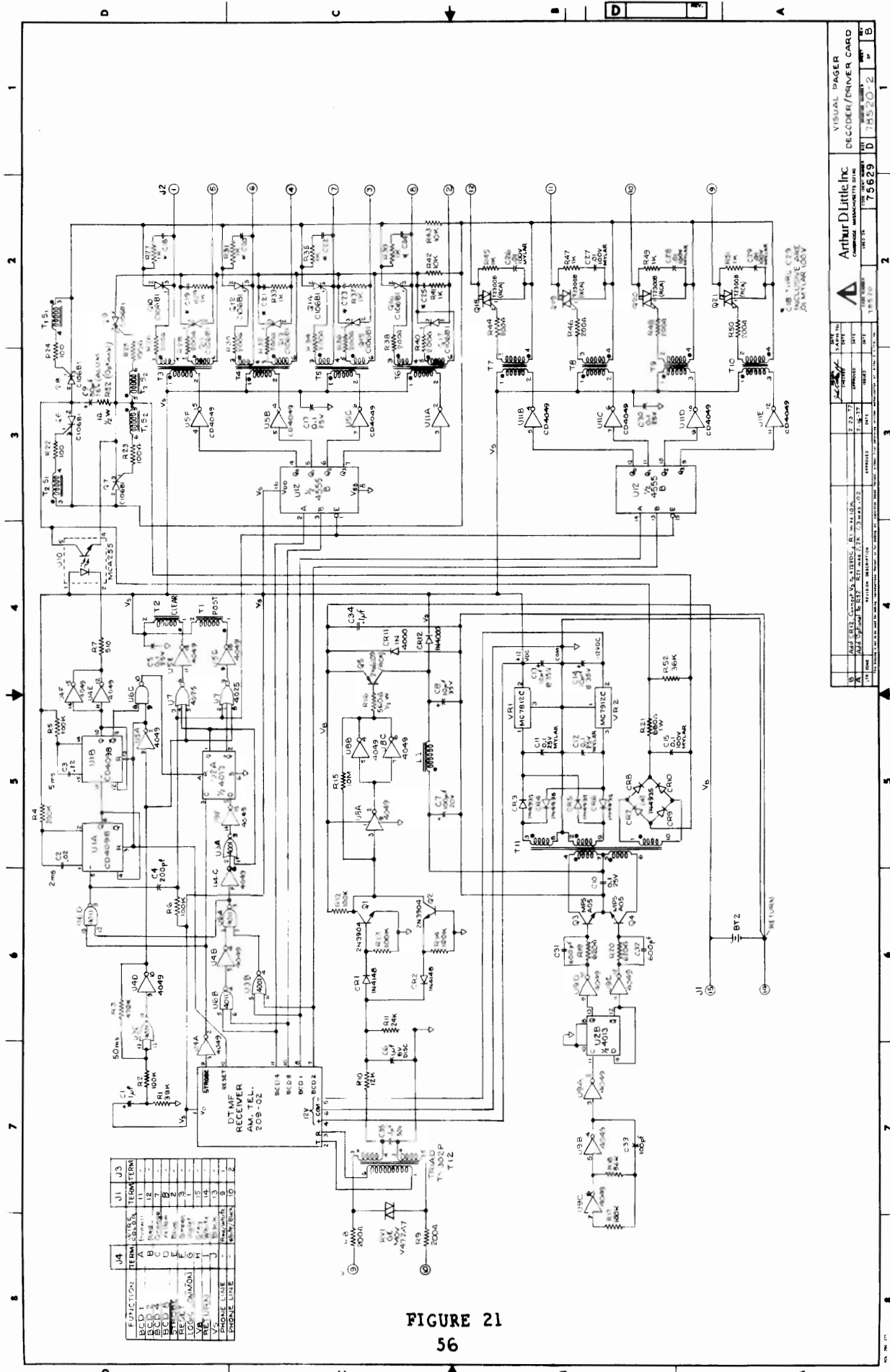
**PARTS LIST**

PREPARED BY \_\_\_\_\_ DATE \_\_\_\_\_ APPROVED BY \_\_\_\_\_ DATE \_\_\_\_\_



APPENDIX III  
VISUAL PAGER DIAGRAM





FUNCTION	ITEM	VALS.	TERMIN.
BCD 1	A	10	11
BCD 2	B	10	12
BCD 3	C	10	13
BCD 4	D	10	14
BCD 5	E	10	15
BCD 6	F	10	16
BCD 7	G	10	17
BCD 8	H	10	18
BCD 9	I	10	19
BCD 10	J	10	20
BCD 11	K	10	21
BCD 12	L	10	22
BCD 13	M	10	23
BCD 14	N	10	24
BCD 15	O	10	25
BCD 16	P	10	26
BCD 17	Q	10	27
BCD 18	R	10	28
BCD 19	S	10	29
BCD 20	T	10	30

FIGURE 21  
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ARTHUR D. LITTLE, INC.  
 100 STATE STREET, CAMBRIDGE, MASSACHUSETTS 02142  
 TEL. 617-452-2000  
 FAX 617-452-2001  
 TELETYPE 617-452-2002  
 CABLE ARTHUR D LITTLE  
 ARTHUR D. LITTLE, INC. IS AN EQUAL OPPORTUNITY EMPLOYER

REVISIONS  
 NO. DATE BY  
 1 11/81 JKL  
 2 12/81 JKL  
 3 1/82 JKL  
 4 2/82 JKL  
 5 3/82 JKL

APPROVED: \_\_\_\_\_  
 DATE: \_\_\_\_\_

ARTUR D. LITTLE, INC.  
 DECODER/INVERTER CARD  
 D 75520-2